3 Device Design and Fabrication

3.1 MIM Structures

Metal-insulator-metal (MIM) capacitor structures can be used to characterize electrical properties of dielectrics. The simplest devices employ uniformly deposited back metal contact and insulator layers and a patterned top contact layer. It is important to use a noble metal for the back contact because other metals will oxidize between depositing the back contact and the insulator, which will affect the measured capacitance of the device. We chose Pt for the back metal layer because ALD alumina is known to nucleate well on Pt; we chose Pt for the top contact metal layer so that the two metal layers would be identical and the capacitance would therefore be independent of voltage.

3.1.1 Fabrication methods:

1) Clean a silicon wafer with a 300 nm thermal oxide.
    a) Insulating silicon or another insulating substrate may be used instead.
2) Put the wafer into an electron-beam evaporator. Deposit 5 nm Ti as a sticking layer, and then 50 nm Pt as the back metal contact.
    a) We deposited metal at 1 A/s using the KJL evaporator; these details are unimportant.
    b) Cr can be used instead of Ti as a sticking layer.
    c) Au can be used instead of Pt for the back metal contact.
3) Cleave wafer into 10 mm square chips with a diamond scribe.

4) Deposit seed layers and an ALD dielectric film as described in §2.
5) Put the chips back onto the electron-beam evaporator chuck. Using clamps or Kapton tape, gently place a shadow mask over but in contact with the chips.
    a) The shadow mask should have a grid of dots; we used a mask with 200 um diameter circular holes at a 1 mm pitch.
    b) Photolithography and liftoff may be used as an alternative to shadow-masking.
6) Deposit 5 nm Ti as a sticking layer, then 50 nm Pt as the top metal contact.
7) Remove mask to reveal finished devices.

3.2 Tunnel Junction Devices

Tunnel junctions can be used to probe characteristics of very thin dielectric films (~ 1 nm). Because thin films typically are more defective than thicker films, it is often desirable to pattern both top and bottom contacts to restrict the junction area to smaller regions than is feasible otherwise. Our design, which features junctions ranging from 16-240 μm^2, is shown in Figure 2.

3.2.1 Device design considerations:

1) Include alignment marks on the pattern for the back contacts. This ensures the junction regions are as close to their nominal size as possible.
2) Electrical measurements will likely be limited by the number of vertical steps/corners on the device (where the dielectric climbs over the step between substrate and back contact) as a result of field focusing. The number and shape of steps over which the junction climbs should therefore be chosen to match the final intended purpose of the thin films.
3) Similarly, the edge length of a given step may have more impact over electrical properties than the total junction area. Performance scaling with both parameters should be examined.
4) Patterning the back contact using liftoff leaves large sidewalls. Sidewalls exacerbate the issues raised by edge steps. Instead, we recommend patterning the back contact by uniform metallization followed by a patterned etch.
5) Metal contacts should be chosen with care. Specifically, any material that readily oxidizes should not be used, as it will introduce an extra oxide layer into the thin film stack. While noble metals are obvious choices, some difficulties with excess dielectric growth and lithography may arise. Additionally, if planning to use a wet etch, metals must be chosen with mutually exclusive etchants (ex. Cr/Pd, Au/Pd)

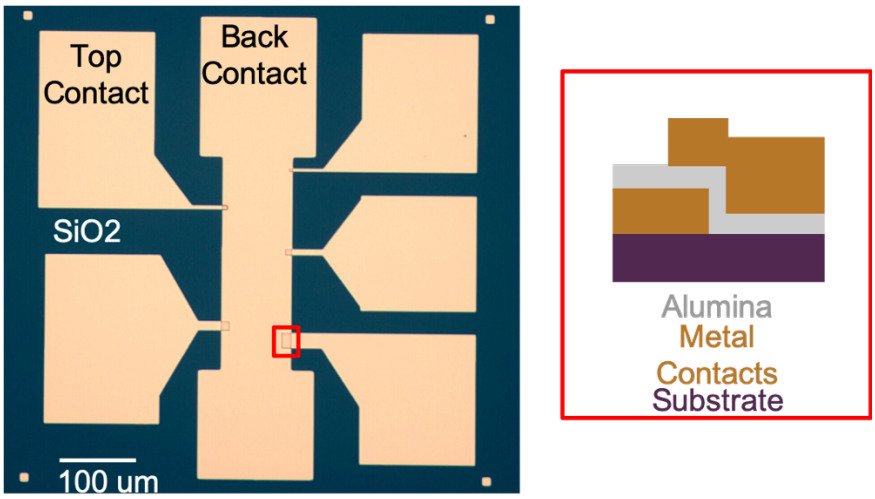

Figure 2. (left) optical micrograph of a tunnel junction device and (right) schematic cross section of the tunnel junction stack. Junction areas range from 16-240 μm^2.

3.2.2 Fabrication:

1) Clean the substrate (see cleaning section)
2) Globally deposit the back contact material as appropriate (see device design considerations). We used 3 nm Cr / 40 nm Pd.
3) Pattern and etch back contacts. We used the following photolithography and etch recipes:
   a) Spin coat AZ1512
   b) Bake 2 minutes on a hotplate at 95ºC (pre-exposure bake)
   c) Expose the inverse of using the ML-3 direct write system at 120 mJ/cm^2
   d) Bake 2 min on a hotplate at 110ºC (post-exposure bake)
   e) Develop 40 s in MF-316 and rinse in two water baths for 20 s each
   f) Remove resist scum with an indirect oxygen plasma ash. Parameters are tool dependent. We used 300W RF power for 15 s in a March Instruments PX-250. Note: excessive ashing can oxidize even noble metals.
   g) Etch as appropriate for your choice of metals. We used 12 s Transene Pd etchant and 30 s Transene Cr etchant.
4) Clean the chip to remove resist (see cleaning section)
5) Deposit ALD film as usual.
6) Clean the chip
7) Pattern the top contacts using the desired technique. We used the following electron-beam lithography and liftoff procedure:
   a) Bake chip at 180ºC for 1 minute (pre-bake; removes water from the surface)
   b) Spin (PMMA) at 4000 rpm
   c) Bake at 180ºC for 2 minutes
   d) Expose top contact pattern with 10 kV beam at 180 $\mu C/cm^2$
   e) Develop for 55 s in 1:3 methylisobutylketone:isopropanol / 20 s isopropanol and immediately dry
8) Deposit top contact metals. We used 3 nm Cr / 60 nm Pd in an electron-beam evaporator.
9) Liftoff excess metal with sonication in acetone and clean as usual (see cleaning section)

4 Characterization

4.1 Physical characterization

4.1.1 AFM

Atomic force microscopy (AFM) provides very precise measurements of step heights, which is valuable to determine the thickness of few-nm ALD films. However, a step between substrate and ALD film must first be created. This is unusually difficult with ALD films because they grow conformally around everything. We accomplished this with a liftoff procedure designed to ensure sharp step edges, which are amenable to AFM.

Procedure for ALD step height measurements:

1) Clean a chip cut from the substrate of interest. As necessary, deposit a seed layer and clean again.
2) Using a needle, drop a small blob of dried PMMA onto the chip (Figure 3A&B).
   a) Hold the needle at a glancing angle so it does not scratch the chip.
   b) Dried PMMA is made by baking a vial of PMMA on a hotplate until it is highly viscous but not solid. Use PMMA in anisole. Bake in a fume hood.
3) Bake the PMMA on a hotplate at 120ºC for 5 minutes to fully evaporate the solvent.
4) Deposit ALD as detailed in section 2.
5) Liftoff the PMMA blob in acetone. This is tricky because ALD will grow conformally around the blob. The final result is show in Figure 3C.
   a) Before putting the chip in acetone, gently scratch the center of the blob with a needle.
   b) Soak the chip in acetone for at least 5 minutes, then sonicate for at least 30 seconds. This helps ensure the liftoff step will be sharp.
   c) Clean the chip with a harsh stream of acetone. This helps remove liftoff fragments from the chip.
   d) Soak the chip in secondary acetone.
   e) Soak the chip in isopropanol.
   f) Blow dry with nitrogen.
6) AFM using the standard procedure for any tool.
   a) We used the Bruker Icon.
   b) For accurate measurement, ensure that the AFM scan direction is across the liftoff step, not along the step, and that the liftoff step is centered in the image.
   c) For accurate analysis of the step height, first correct the image using a first order plane fit to the substrate side of the step. Then make a histogram of the heights in the image. The heights should be bimodally distributed. One peak corresponds to the substrate, the second peak corresponds to the ALD film. The ALD thickness is given by the distance between the center of the two peaks.

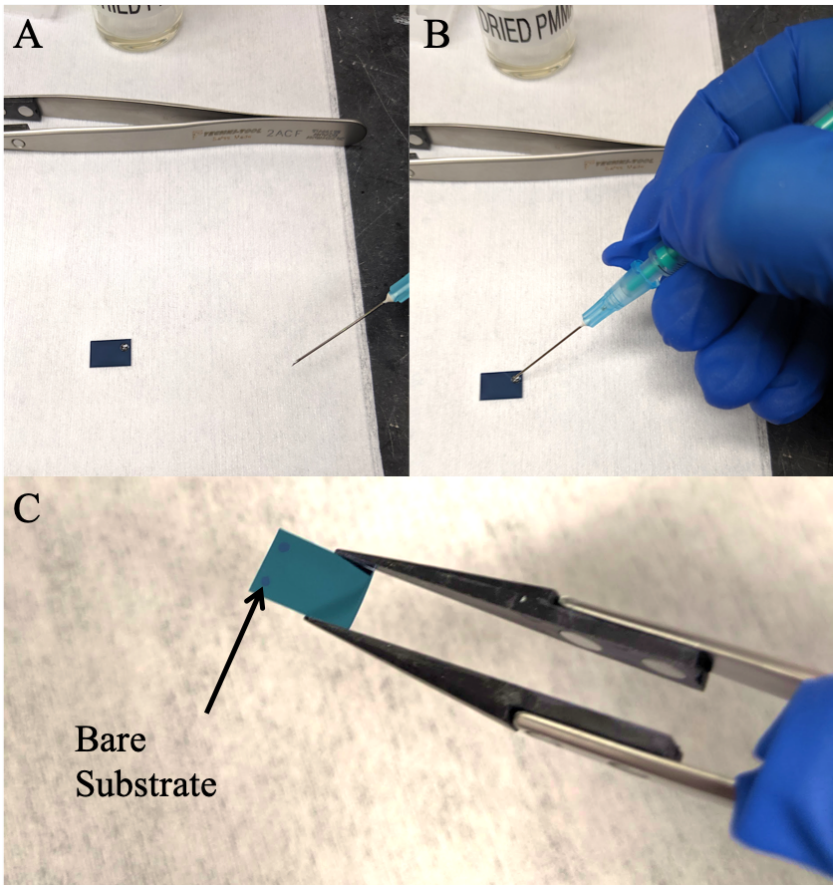

Figure 3. Using drop-cast PMMA for ALD liftoff. A) Using a needle to place a small blob of dried PMMA on a silicon chip. B) Silicon chip with a small blob of PMMA. C) Silicon chip after ALD deposition and PMMA liftoff. The regions of bare substrate that were masked by PMMA during the deposition are indicated.

4.1.2 Ellipsometry

Ellipsometry is a fast and simple method that provides information about the thickness of thin films. However, ellipsometers have poor spatial resolution and therefore average information over their ~1mm^2 spot size. As a result, a sample with roughness on the order of the film thickness is not a good candidate for ellipsometry.

A general procedure can be found at https://snf.stanford.edu/SNF/equipment/characterization-testing/woollam-m2000. Data analysis can be performed either within the cleanroom at the Woollam or outside of the cleanroom, at the computer in the SNF staff cubicle area.

We recommend the following procedure for measuring the thickness of ALD films with ellipsometry:

1) Measure bare substrate before any seeding or ALD deposition according to the tool manual.
2) Analyze the data to determine a model for the substrate. Fit n and thickness (not k) and save any relevant substrate thicknesses (i.e. native SiO_2 on bare Si) and optical models.
3) Deposit seed layers and ALD films as needed.
4) Measure the substrate/film heterostructure.

5) Analyze the data to determine ALD film properties. Import the saved thickness and optical model of the substrate from step 2. Add a layer of the ALD film material; fit n and thickness but do not fit k.

4.1.3 X-ray photoelectron spectroscopy

X-ray photoelectron spectroscopy (XPS) determines the chemical composition of a film by irradiating the sample with x-rays and measuring the resultant photoelectrons. With proper care, XPS can give quantitative chemical information accurate to a few percent, and provide a wealth of information about both chemical bonding states. It can further elucidate differentiate superficial and bulk chemistries with depth or angled profiling. XPS has essentially no spatial resolution, as it averages signal over an ~200x200 μm in-plane area. It is a mostly-surface sensitive technique with an interaction depth of 5-10 nm depending on the sample. It should be noted that neither hydrogen nor helium can be detected with XPS.

Tool information for the PHI VersaProbe 3 in SNSF can be found at https://snsf.stanford.edu/equipment/xsa/xps_vp3.html. Data analysis can be performed with MultiPak within SNF or with CasaXPS using a license available to Stanford affiliates.

We suggest the following procedure for collecting XPS data, but many variations could be useful:

1) Full spectrum that includes all potentially relevant peaks
2) Sputter off any surface layer. Begin with 1.5 nm.
3) Repeat the full spectrum to confirm the surface was properly cleaned.
4) Focused scans of all important peaks.
5) Return to (2) and repeat as desired.

4.2 Electrical characterization

Current-voltage (I-V) and capacitance-voltage (C-V) measurements can be performed using the Micromanipulator6000 in SNF ExFab. The Micromanipulator manual can be found at https://snf.stanford.edu/SNF/equipment/characterization-testing/Micromanipulator6000/micromanipulator6000. Although the micromanipulator is capable of four-point measurements, the protocols described below only require two probes.

4.2.1 Load sample

1) Enable the tool on Badger.
2) Raise the enclosure screen.
3) Place the sample on the sample chuck.
4) Turn on the vacuum to secure the sample.
5) Use the stage controls to move the sample into position (i.e. so the region of interest is visible in the microscope.
6) Move the probes close to position by hand and make fine adjustments with the knobs on the sides of the probes.

4.2.2 Make contact to the back contact

1) Attach one probe to SMU3, and the other to SMU4.
2) Move both probes over the back contact region, close to top contact of interest.
3) Lower the probes into contact with the sample and scratch both probes through the ALD film (Figure 4A).
4) Run an I-V sweep from 0V→100 mV→0V in steps of 1 mV with a compliance current of 1 mA.
5) Check to see if your measured resistance agrees with your expectations for the back contact's resistance (~10 Ohms for a metal).
6) If the measured resistance is too high, one or both of your probes is not in contact with the back contact. Scratch a little further.
7) Repeat steps 4-6 until both probes are in contact with the back contact.
8) Lift the probe connected to SMU3, leaving the other behind.

4.2.3 Make contact to the top contact

1) Move the SMU3 probe directly over (not touching) the top contact of interest.
2) Start a Cs-Rs measurement through CMU1 (this is the same as SMU3) at 1 kHz excitation, from -100 mV→100 mV→-100 mV in 1 mV steps. Line self-capacitance should be ~400 fF.
3) Lower the probe slowly while watching the C-V measurement. When the measured capacitance jumps to its expected value (order 100 pF for 10 nm AlOx dielectrics and MIM structures described in §3.1), stop lowering the probe. The final probe positions are shown in Figure 4B.
4) Gently turn off the microscope light, being careful not to bump anything.
5) Ensure the measured capacitance did not change during step 4. If it has changed, turn the light back on and return to step 3. Otherwise, proceed.
6) Slowly close the enclosure.
7) Ensure the measured capacitance did not change during step 6. If it has changed, turn the light back on, open the enclosure, and return to step 3. Otherwise, report the measured capacitance.
8) After determining the capacitance, determine the breakdown voltage of the device by measuring the I-V characteristic of the device starting at 0 V and sweeping upwards until breakdown. At the breakdown voltage, the device will suddenly become an electrical short.
9) Repeat as needed with additional top contacts.

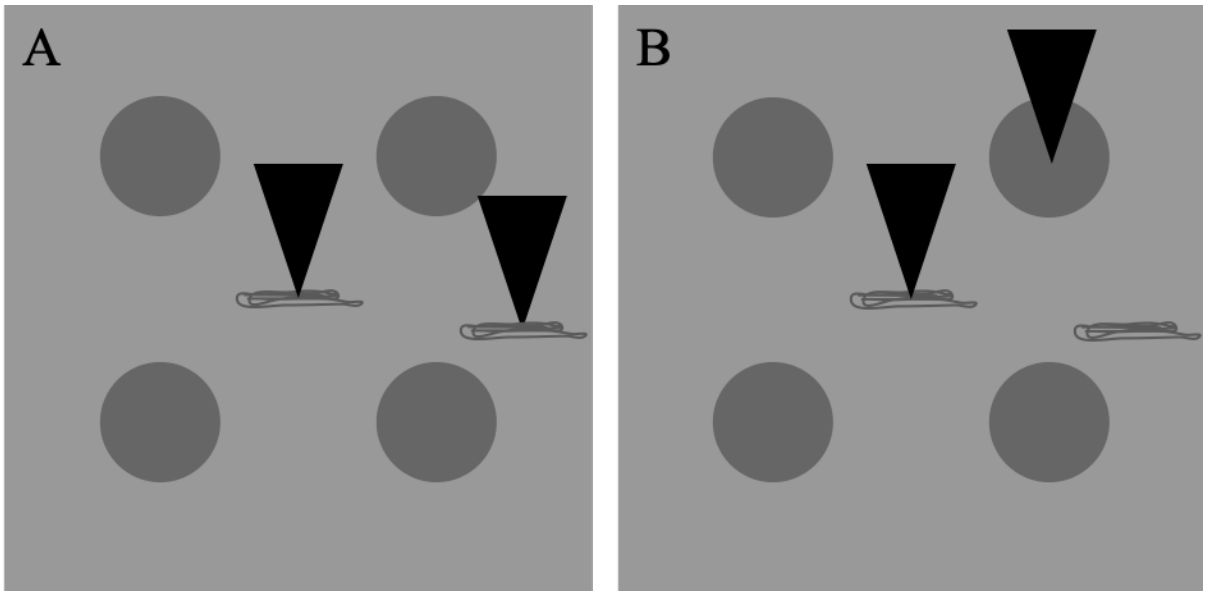

Figure 4. Schematic representations of the steps to contact MIM devices with a micromanipulator. Black triangles represent micromanipulator probe tips, grey dots represent metallic top contacts. A) Ensuring good electrical contact to the back contact by scratching both probes through the ALD film. B) One probe moved to the top contact for dielectric measurements.

4.2.4 A note on capacitance measurements

We recommend modeling MIM structures as a capacitor and a resistor in series. On the Micromanipulator, this is done by selecting Cs-Rs measurement (one of the standard available measurements). We recommend performing this Cs-Rs measurement through CMU1 at 1, 10, and 100 kHz excitation, from -100 mV→100 mV→-100 mV in 1 mV steps. Within this voltage range, most dielectrics should have a flat and linear C-V relationship. Data can be exported and analyzed in your preferred software.

4.2.5 A note on breakdown measurement

After measuring the capacitance of the MIM structure, breakdown I-V measurements can be performed. Note: this will irreversibly affect the local dielectric, so all other measurements should be completed first. We recommend 0V→20 V→0V sweeps in 5 mV steps with a 100 mA compliance current. Measured current should begin as pA noise around 0 A. The measured current will increase exponentially in the pre-breakdown regime. At the dielectric breakdown voltage, the current will suddenly jump to the compliance limit. Data can be exported and analyzed in your preferred software.