Fabrication of an Etched Silicon Platform with Applications in Uniform Dissection of Biological Samples

ENGR 241 Winter Quarter Standard Operating Procedures
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Summary

This document contains standard operating procedures (SOPs) for the following processes:

1. Fabrication of oxide hard mask for deep silicon etching.
    a. Deposit oxide with **CCP-DEP**
    b. Pattern photoresist with **Heidelberg**
    c. Wet etch oxide and strip photoresist using **wbflexcorr** benches
2. Tapered etch method for blade formation using **PT-DSE**
3. Through-hole etching using **PT-DSE**
    a. Backside oxide deposition using **CCP-DEP** for etch stop
    b. Bonding wafer to carrier using **Crystalbond** with **Headway Spinner**
    c. Lifting off devices

The procedures were used to arrive at an array of blades separated by through-holes. However, beyond specific target design, these operating procedures are valuable for successfully conducting any large-scale silicon etching in the PT-DSE.

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1 Oxide Hard Mask for PT-DSE

For applications using short length isotropic etch times (i.e., the 'ETCHB' step in the standard 'DSE_FAT' recipe) like the conventional Bosch deep silicon etching in the PT-DSE, hard baked photoresist masks may suffice. However, we quickly discovered that for our purposes, which require deep and wide etches and non-traditional long isotropic etch times, photoresist etch masks caused rough etch surface finishes (Fig. 1A). Likely, excess polymer gas in the chamber from continuous, low-bias power etching functioned as micromasks and rendering our structures rough. Grassing caused by micromasking was also observed in etching for through holes (see procedure 3: Through-Hole Etching). Thus, we opted to use oxide hard masks for our application, and we encourage anyone etching a wide and deep feature to do the same.

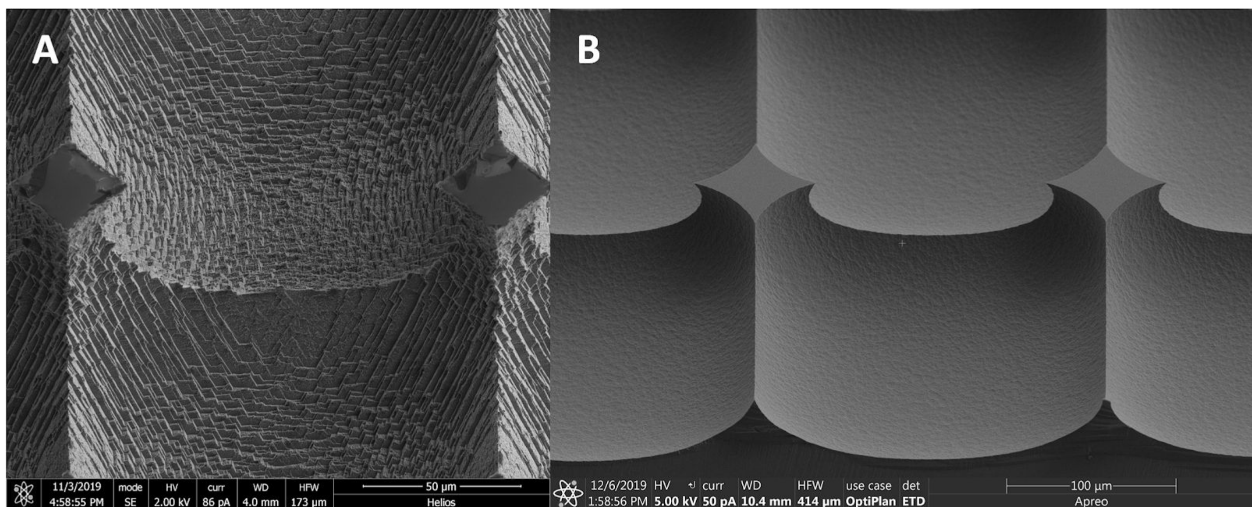

Figure 1: (A)Rough surface finish when using 1.6 µm thick SPR 3612 photoresist mask for long isotropic etches in the PT-DSE. (B) Surface finish when using a 1µm thick oxide mask and the same etching recipe as in A.

1.1 Deposit oxide with CCP-DEP

1. Grow oxide mask using PlasmaTherm CCP-DEP PECVD system for oxide on silicon at 350 °C standard recipe for the amount of time corresponding to your desired oxide mask thickness.
    - To get an adequate mask for our purposes (blade formation followed by through-hole etch), we required at leasta 3 µm thick oxide mask, which required ~45 minutes of deposition.
    - Refer to the log book for the etch times and thicknesses of previous users
2. Measure oxide mask thickness using the Nanospec2 (silicon oxide on silicon).
    - Note this thickness to later check oxide etch rate after a round of PT-DSE etching.
3. Optional: annealing (between 400 and 1000 ℃) will harden the mask and present stress build up in masks left sitting for extended periods of time before use [1].

1.2 Pattern photoresist with Heidelberg

4. Prime wafer with HMDS (hexamethyldisilizane) to improve photoresist adhesion in the YES oven for 20 minutes, following the standard protocol.
5. Use the SVGcoat to spin and soft bake SPR3612 photoresist @1.6 µm over the oxide layer to serve as a BOE etch mask.
    - To avoid wafer transfer issues on any SVG track, always reset the index
6. Load the desired mask file into the Heidelberg and after running a test exposure, pattern your wafer with -2 µm defocus and 85 mJ/cm^2 dose.
    - For reference, we constructed our mask with the following boolean operations in the design editor:

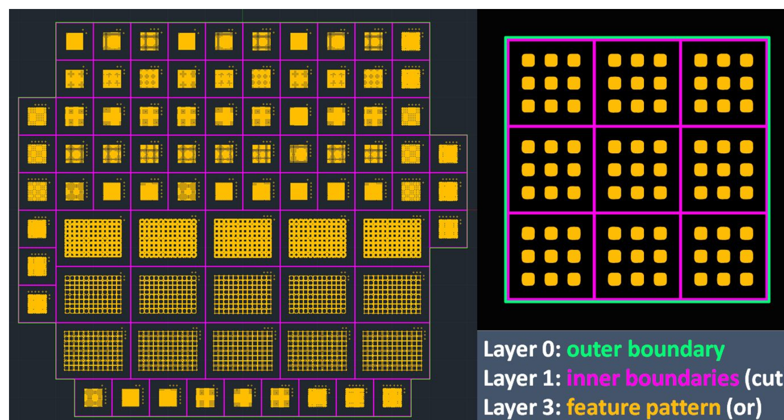

Figure 2: Actual mask design in .dxf format (left) and zoomed in schematic showing boolean operation (right) used to create the job file on the Heidelberg, where all colored areas where exposed

7. Use the SVGdev to develop and hardbake the photoresist.
8. Descum the wafer with the Technics plasma asher to prepare the surface for oxide wet etching.

1.3 Wet etch oxide and strip photoresist using wbflexcorr benches

9. Isotropic wet etch the wafer with 6:1 BOE (34% Ammonium fluoride (NH_4F), Hydrofluoric acid 7%, 59% water) to pattern the oxide, using photoresist as a mask for 35 minutes, followed by 3 DI water rinses.
    - 6:1 BOE etches oxide at ~0.1 µm/min with high selectivity
10. Strip the photoresist with Piranha (70% - 90% sulfuric acid (H_2SO_4), hydrogen peroxide(H_2O_2) for ~10 minutes @ 120 °C, followed by 6 DI water rinses.
11. The wafer now has a silicon oxide mask and is ready for dry etching using the PT-DSE

2 Tapered Blade Formation Using PT-DSE

For etching silicon using the PT-DSE, create or adapt a new recipe that includes at least the following main steps will be 1: Gas stabilization (Gs), 2: Light (Lt), 3: Etch, 4: Pump Detach. If creating a new recipe, be sure to (1) rename any steps you are editing with your initials (2) save the overall recipe with your initials. IMPORTANT NOTE: Editing steps in a recipe WILL change all other instances where the steps are referenced (e.g If EtchA_SK modifies the bias voltage of step A and 'test_recipe1' and 'test_recipe2' both call EtchA_SK, both recipes will see the edit to EtchA_SK even if you edited the step only in context of 'test_recipe1').

If the etch is isotropic, the ICP Match Tune Setpoint Position in the gas stabilization step will need to be changed to a setpoint of around **72.0.** If the etch is anisotropic and requiring cycling, the setpoint is likely around **65.0.** If you do not change the ICP Match Tune Setpoint Position in GS there will likely be an error with reflected/delivered ICP power.

Best practice is to test a new recipe for a few seconds on a dummy wafer. First, put the tool in maintenance mode, and click to transfer the material manually from the load lock to the chamber. Then, place the tool back into production mode and monitor the key parameters (ICP reflected power low (< 50W), correct gas ratio, etc).

The SOP below describes how to etch blades of different angles with this tool.

2.1 Creating the recipe

1. Open the recipe DSE_FAT_EBTr and save the recipe under a new name (e.g. DSE_FAT_EBTr_XX). Modify the recipe to delete the two pump detach steps at the end.
2. Save the step DSE_FAT-GS under a new name (e.g. DSE_FAT_GS_XX). Modify the step such that the ICP Match Tune Setpoint position is 72.0
3. Save the step DSE_FAT-Et B under a new name (e.g. DSE_FAT-ET B_XX). Modify the following parameters: (1) Process Time Setpoint to 100s (2) C4F8 to 50 (3) Gas 1 Dump Valve Direction to #To PM (4) Gas 2 Dump Valve Direction to #To PM
    - In our recipe, we set the isotropic etch time to be 100 s and introduced a small amount of passivation (50 sccm of C4F8 gas).
    - The time of isotropic etching can be varied as can the amount of C4F8.
4. Append those steps to the DSE_FAT_EBTr_XX. You should have the following steps in your recipe. Steps are listed in order: (1) DSE_FAT-GS (2) DSE_FAT-Lt (3) DSE_FAT-Dep (4) DSE_FAT-Et A (5) DSE_FAT-Et B (6) DSE_FAT-EBTr (7)DSE Fat-Pdw (8)DSE FAT_GS_XX (9) DSE_FAT-Lt (10) DSE_FAT-ET B_XX (11) DSE_FAT_Pdw
5. Create a new recipe 'Pump Detach_XX' that contains the two pump detach steps that you have deleted from DSE_FAT_EBTr.

6. In the ‘Editors’ tab, click on ‘Loop Editor.’ Since we want to repeat the BOSCH portion of the etching n times, click on the last step of the recipe and set the number of loops accordingly. If you have set the loop correctly, all the steps that will be looped (e.g. DSE_FAT-Dep / DSE_FAT-Et A / DSE_FAT-Et B / DSE_FAT-EBTr) will be indented on the ‘Recipe Steps’ table on the left hand side of your screen.

2.2 Running the recipe

7. Pump down the load lock
8. Place all chambers of the tool in Maintenance Mode
9. In the ‘Maintain’ tab, transport the wafer from AL_BML 1 to PM_PM1_ML1
10. Once the wafer has been transported into the process module, put the process module (PM) into production mode
11. Go back to the system tab and press ‘Start Job’
12. Once the job status changes from ‘Active’ to ‘Idle’ you know that your process is complete
13. Click on ‘Start Job’ N times, where N is the number of bosch + iso cycles you are interested in to form the blades. A tally of the number of times you click ‘Start Job’ is also recorded in the ‘Data Log’ tab.
14. Once you have finished N iterations, run the Pump Detach_XX steps
15. Put all chambers back into Maintenance Mode and transport the wafer from the process module back to the load lock
16. Vent the load lock and remove your wafer

2.3 Wafer cleaning

We have found that cleaning the wafer after etching the blades reduces the amount of accumulated scum. There are multiple ways to descum, two recipes on (1) Matrix (2) Samco are below:

- Most of the Matrix recipes are identical (2 min O2 plasma clean). In specific, we used Nancy1 > 19050210.04 > LONG_STR0.01 > LONGSTR.RCP
- On the SAMCO, we used 15 sccm of O2, 50 W power, 15 Pa of pressure for 2 minutes to descum the wafer.

3 Through-Hole Etching Using PT-DSE

We used a single mask approach for creating blades and etching the through-holes because we found that an oxide mask suspended between some pillars was sufficient for protecting edges during the etching of the through-holes as long as the mask did not collapse (mask collapse discussed in Appendix of the report that complements this SOP document) (Fig. 3A). While mask stability was sufficient, we reiterate that no less than 3 μm thick oxide should be used as a PT-DSE hard mask for large scale etching similar to ours.

With deep, through-hole etching it is necessary to mount the wafer on a carrier wafer so that no vacuum is released on the backside of the wafer. Crystalbond offers a strong attachment to a carrier wafer with good heat conduction properties necessary for the PT-DSE. However, much like the problem with using photoresist as a mask, as soon as Crystalbond is exposed to plasma, excess polymer in the chamber is produced and micromasking can lead to grassing. To mitigate this, we added an oxide etch stop on the backside of the wafer prior to mounting it to the carrier.

3.1 Backside oxide deposition using CCP-DEP

1 um of oxide was deposited on the backside of the wafer after the wafer front-size oxide mask was fully processed. The oxide on the back acted as an etch stop (to ensure we were not etching through the crystal bond and causing the crystal bond to redeposit into the PT-DSE chamber). Backside oxide deposition was done on the CCP-DEP for approximately 15 minutes at 350 ℃. We confirmed that 1 um oxide was deposited using the Nanospec (oxide on silicon). Please refer to other recipes in the binder to explorate based on the most recent rate of deposition.

3.2 Bonding wafer to carrier using Crystalbond

1. Crystalbond 509 is crushed up with a mortar and pestle and mixed in a solution of 80 parts acetone to 20 parts Crystalbond by weight (e.g., 101 mL of acetone, assuming 0.791 g/mL density at room temperature, and 20 g of crushed Crystalbond.
2. Turn on hotplates to allow them to get to set temperatures of 90 ℃ and 125 ℃.
3. Program the Headway2 spinner:
    - Step 1: 500 RPM for 10 s with 100 RPM/s ramp up
    - Step 2: 1500 RPM for 30 s with 500 RPM/s ramp up
    - Step 3: 0 RPM for 0 s with 100 RPM/s ramp down
4. Set the carrier wafer on the chuck and apply a liberal amount of Crystal bond solution to the surface.
    - We found that the film is poorly distributed if all parts of the wafer surface are not wetted with Crystalbond to start.
5. Allow acetone to evaporate for 5 minutes at room temperature (should see a slight color change).
6. Heat wafer for 1 minute on the 90 ℃ hotplate.
7. Heat wafer for 3 min on 125 ℃ hotplate.
    - At this temperature the crystal bond is liquid and can flow a bit during placement of the patterned wafer.
8. Place the patterned wafer on top and slide it to center on the carrier wafer.
    - Use the flats to help with alignment.
    - You can heat again at 125 ℃ for fine adjustments.
    - Allow 4 minutes for good contact.
9. Optional: we washed away any excess Crystalbond on the backside of the carrier wafer and the topside of the patterned wafer to avoid polymer sticking to the PT-DSE bottom-side wafer chuck or top-side vacuum chuck.

10. Allow 30 minutes before etching.

3.3 Morphing bias voltage for clean through-etch

Any through-wafer dry etch (DSE_FAT or DSE_Nano) can be limiting and introduce bottom grassing as the etch deepens into the wafer. We noticed that the through-hole at the bottom was significantly smaller in dimension than the mask opening (Fig. 3). To address the issue of decreasing lateral etch rate with etch depth, we increased the bias in the etch A step from a nominal value of 250 V gradually to 400 V. Our morph curve parameter was 0.3, since we wanted the majority of our bias voltage to be towards the end of our through-etch. Note: We observed that there was a difference between the setpoint and actual bias voltage each step. The controller overshoots/ undershoots, but across the given number of steps, it will eventually reach the endpoint.

1. Save DSE FAT-Et A and as a new step with your desired name. (e.g. DSE FAT-Et A_Morph). Save DSE_FAT_EBTr with a new name (e.g. DSE_FAT_EBTr_Morph) and include your new Etch A step.
2. In the 'Loop Editor' tab, click on the step that you want to morph, set the corresponding start setpoint and end setpoint.
    - Modify the morph curve according to whether you want the morphing to be delayed (between 0.1-0.9), linear (1.0), or rapid (1.1-10.0).
    - The software will use this morphing curve and distribute it over the number of loops of your step.

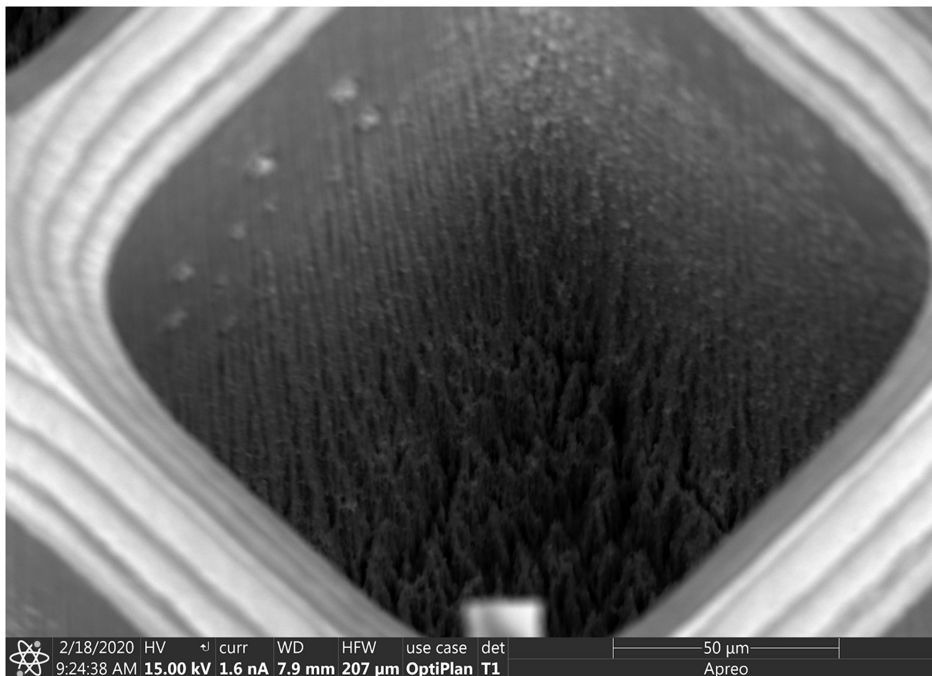

Figure 3: Example of grassing occurring during through-hole etching that impeded the etching process. Morphing the bias voltage as the etch went deeper was the best solution to clear this grassing for successful through hole etches

3.4 Isotropic etching to clean bottom grassing

To address the issue of bottom grassing, we appended 80-100 s of isotropic etching at the end of our through-etch. Only the etching gas SF_6 (no passivation gas C_4F_8) was present in the process module during this final isotropic etch.

3.5 Post processing and lifting off devices

To make processing our wafer easier we decided to include device borders in our etch mask so that we would not need to dice the wafer. This is possible since our device is fabricated on a carrier wafer and adhered with Crystalbond.

1. Etch the oxide mask and exposed backside oxide through the through-holes with a BOE etch as described in section 1.3. However, etch for only 12 minutes. Follow with 3 rinses in DI water.
    - Note: some devices might start to lift off during the BOE etch.
2. To lift off the remaining devices, place the wafer in an acetone bath in a sonicator for 5 minutes (you will start to see devices lifting off) or without a sonicator for 8 hours.
3. Optional: To remove any remaining oxide on the back side of the devices that were covered in Crystalbond, repeat the BOE for another 12 minutes.

Figure 4: A wafer before (Left) and after (Right) device lift off.

Bibliography

1. Fu, J., Shang, H., Li, Z., Wang, W., and Chen, D. (2017). Thermal annealing effects on the stress stability in silicon dioxide films grown by plasma-enhanced chemical vapor deposition. Microsyst. Technol. *23*, 2753–2757.