A Low Temperature, Low Stress SiGe Process

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ABSTRACT

In this project, we developed a low temperature ($\leq 450^0$C) silicon-germanium (SiGe) process using the Thermcopoly1/2 furnaces at SNF. Low stress (≤ 100MPa) poly SiGe has been successfully demonstrated with a deposition temperature below 450^0C and desired Si to Ge content ratio. Our SiGe deposition process is CMOS compatible and can enable a number of applications for microelectromechanical systems (MEMS), especially monolithic integration of MEMS on top of CMOS. Low stresses in our deposited SiGe have been confirmed by patterning the SiGe into various MEMS structures, (i.e., cantilevers, Guckel Rings). Functional nanoscale electromechanical relays with B doped SiGe have been demonstrated. Additionally, our recipe can also be used to deposit Ge below 400^0C, which can be etched by H_2O_2 and provides alternative choice for MEMS sacrificial layers.

1. INTRODUCTION

Monolithic integration of microelectromechanical systems (MEMS) on top of CMOS substrate is highly desirable for high performance and low power applications (Fig. 1) [Chong 09, Chen 10]. However, integrating MEMS on top of CMOS requires a low temperature MEMS process (<450^0C) [Sedky 02].
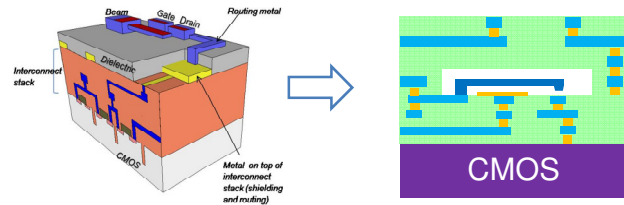

Figure 1. Monolithic integration of nanoelectromechanical relays on top of CMOS.

Silicon is a widely used material for surface micro-machined MEMS due to its outstanding mechanical and electrical properties. However, in order to achieve low stress in the poly Si film, a temperature higher than 800^0C is needed [Zhang 98]. Previously, functional nanoelectromechanical (NEM) relays using poly-silicon as a beam material have been demonstrated [Parsa 11]. The poly-Si is deposited at 580^0C using Thermcopoly and then annealed at ~1000^0C using RTA. However, due to the high temperature during poly-Si deposition, this NEM relay process is not CMOS compatible.

It has been reported that alloying Ge with Si can effectively reduce the deposition temperature to a CMOS compatible level (~450^0C). The deposited SiGe film exhibited low stress (10MPa compressive), which is good for building microelectromechanical structures. After Boron doping, SiGe would also have good electrical conductivity [Sedky 02]. Additionally, amorphous Ge can be etched in H_2O_2, which could be used as a low temperature MEMS sacrificial layer material instead of SiO_2.

Therefore, in this work, we developed a CMOS compatible, low-temperature and low-stress SiGe process at SNF, which enables a wide range of MEMS applications, especially the integration of MEMS with CMOS, and providing alternative choice of MEMS/NEMS sacrificial materials to the MEMS community.

2. Materials and Methods

Our target was to develop a SiGe process with a deposition temperature $\leq 450^0$C and stress ≤ 50MPa using Thermcopoly1/2.

Before SiGe deposition, we prepared a number of wafers with 1.5um SiO_2 on 4-inch silicon substrates. Both LTO and thermal oxide were deposited for comparison. The SiO_2 layer could help us measure the thickness of the deposited SiGe film and also serves as a sacrificial layer when designing MEMS/NEMS structures using the deposited SiGe film.

Based on discussions with SNF staff and users who frequently use Ge, we learned that Ge and possibly SiGe would require a Si seed layer to nucleate. Hence, we deposited ~2nm Si seed layer on half of our wafers using Innotec or Thermcopoly. The Thermcopoly Si seed layer still required high temperatures (550^0C) but was used as a proof of concept.

Three gas precursors were available for SiGe deposition on Thermcopoly: SiH_4, GeH_4, and B_2H_6 (optional for Boron doping). Based on our initial literature search [Lowe 07], the capability of the Thermcopoly furnaces, and our target experimental goals, we chose an initial set of processing parameters and ranges as shown in Table 1. These parameters can be edited in the PSIGEB recipe on Thermcopoly. Since it's time-consuming for Thermcopoly to cool down to our targeted deposition temperature, a standby recipe (STBY450) has been created to put the Thermcopoly tube into 450^0C standby mode.

Table 1: Processing parameters and their values in our experiments.

Parameter	Value
Temperature	400^0C, 450^0C
Pressure	300, 400 mTorr
SiH4 flow rate	0-150sccm
GeH4 flow rate	0-50sccm
B2H6 flow rate	0-20sccm

As an example, the runs we accomplished are listed in Table 2. Due to the limitation and control accuracy of temperature control on Thermcopoly, we chose 400^0C and 450^0C as our main deposition temperature. Run #1 and #2 were pure silicon deposition with/without B doping at 450^0C. Run #3 targeted B doped SiGe with 2:1 Si to Ge ratio, which matched the recipe from literature except for a different B precursor [Lowe 07].

Run#4 and #5 were pure Ge deposition with and without B doping at 450^0C. Run #6 explored the deposition rate of Si at 400^0C. Run #7 targeted the similar deposition as Run #2 under lower deposition temperature (400^0C). Run #8-#9 tested the influences of chamber pressure. As we will show later in this report, we obtained SiGe depositions from Run #2, 3, and 6, 7, which are highlighted in Table 2. Since the characterization took longer than expected (to measure thickness, composition, resistivity, and stress), we focused most of our efforts on characterizing films 2, 3, and 4.

Table 2: Examples of completed SiGe deposition runs.

Run #	Pressure (mTorr)	Temperature (C)	SiH_4 (sccm)	GeH_4 (sccm)	B_2H_6 (sccm)
1	400	450	150	0	0
2	400	450	100	50	0
3	400	450	100	50	20
4	400	450	0	50	0
5	400	450	0	50	20
6	400	400	100	50	0
7	400	400	100	50	20
8	300	450	150	0	0
9	300	450	100	50	0

3. Results

3.1 Deposition Rate

We specifically measured the thickness of the deposited SiGe and Ge films obtained from Run #3 (400mTorr, 450^0C, SiH_4-100sccm, GeH_4-50sccm, and B_2H_6-20sccm) and Run#4 (400mTorr, 450^0C, GeH_4-50sccm). The SEM pictures of the wafer cross sections of these two depositions are shown in Fig. 2a and 2b. For both runs, the total deposition time was 1 hour. As shown in Fig. 2a, the SiGe film from Run #3 is polycrystalline, and the thickness is 550nm. However, as in Fig. 2b, the Ge film out of Run #4 is amorphous, and is 400nm thick. Comparing the surface of these two films, we can see that the amorphous Ge film surface is much rougher than the SiGe film. The deposition rate for SiGe (Run #3) is 92Å/min, and the Ge deposition rate for Run#4 is 67Å/min. The deposition rates are listed in Table 3.
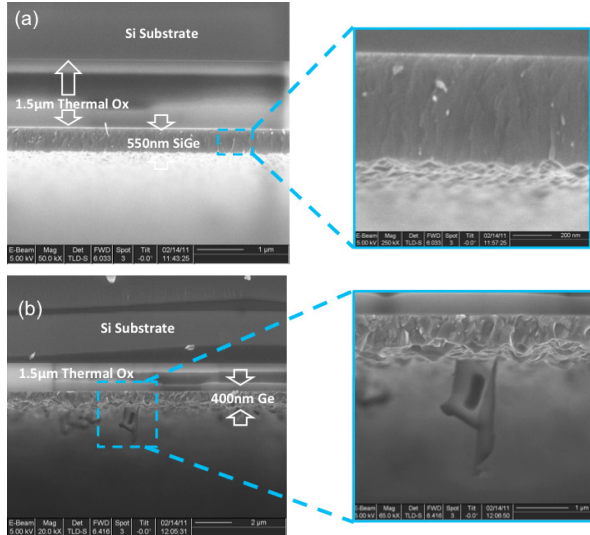

Figure 2: SEM pictures and the measured film thickness of two deposited films after 1-hour deposition: (a) Poly SiGe deposited at 450^0C from Run #3; (b) Amorphous Ge after an hour deposition (Si seed layer required).

Table 3: Measured deposition rates for SiGe and Ge films.

Film	Deposition Rate	Conditions
SiGe	92Å/min	400mTorr, 450^0C, SiH_4-100sccm, GeH_4-50sccm, and B_2H_6-20sccm
Ge	67Å/min	400mTorr, 450^0C, GeH_4-50sccm

3.2 Film Composition

To analyze the composition of the SiGe and Ge films, we conducted X-ray Photoelectron Spectroscopy (XPS) and Auger measurements at SNL.

Figure 3a and b shows XPS measurement results for SiGe film deposited from Run #3 and Ge film deposited from Run #4. Both measurements were conducted after sputtering into the sample. There is usually carbon and oxygen present on the surface so measuring the sample after sputtering gives a much better idea of the film composition.

Using the thickness measurement from the cross sections (Fig. 2) and the compositional data from the XPS and Auger analysis (Fig. 3 and Fig. 4), the thickness was also measured using the Woollam ellipsometer. An initial layer stack of 100Å surface roughness, 10000Å Si_xGe_{1-x} where x=0.35, 15000Å thermal oxide, and 1mm Si substrate were used. A reasonable fit for the data was found with 115Å surface roughness, 10213Å Si_xGe_{1-x} where x=0.342, and 15112Å thermal oxide (Fig. 5). The optical constants for the SiGe layer were fitted while all other optical constants were fixed.

3.3 Sheet Resistance

To confirm the B doping effect for the SiGe films, we measured the sheet resistance for both the doped SiGe and undoped SiGe under various deposition temperatures, which are listed in Table 4. The sheet resistance was measured at 5 different sites per wafer.

As shown in Table 4, both doped SiGe films under 450^0C and 400^0C showed low sheet resistance (~20Ohm/□), indicating the effective Boron doping during the deposition. However, the undoped SiGe film showed a sheet resistance up to 6.81 $x10^5$ Ohm/□, which is much higher than the doped SiGe.
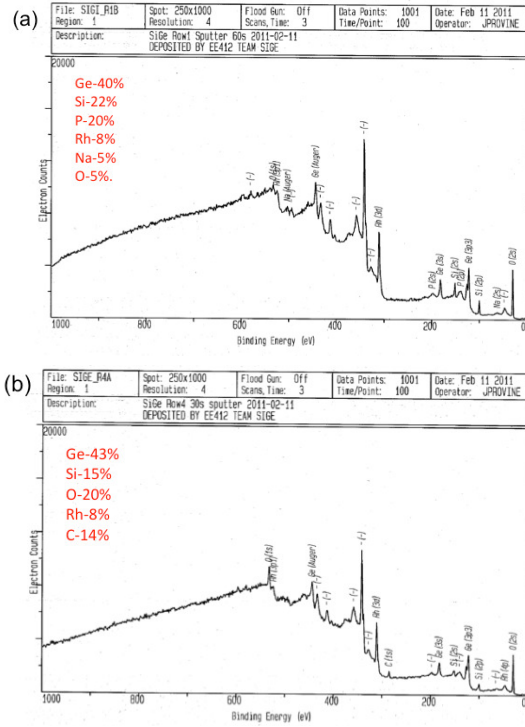
Figure 3: Film compositions measured using XPS for the deposited SiGe and Ge films: (a) SiGe film deposited under 400mTorr, 450^{0}C, SiH$_4$-100sccm, GeH$_4$-50sccm, and B$_2$H$_6$-20sccm; (b) Ge film deposited under 400mTorr, 450^{0}C, GeH$_4$-50sccm.
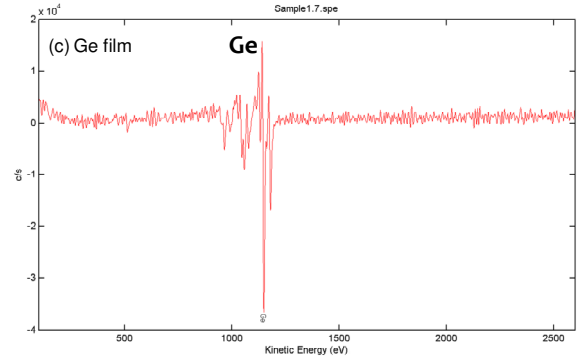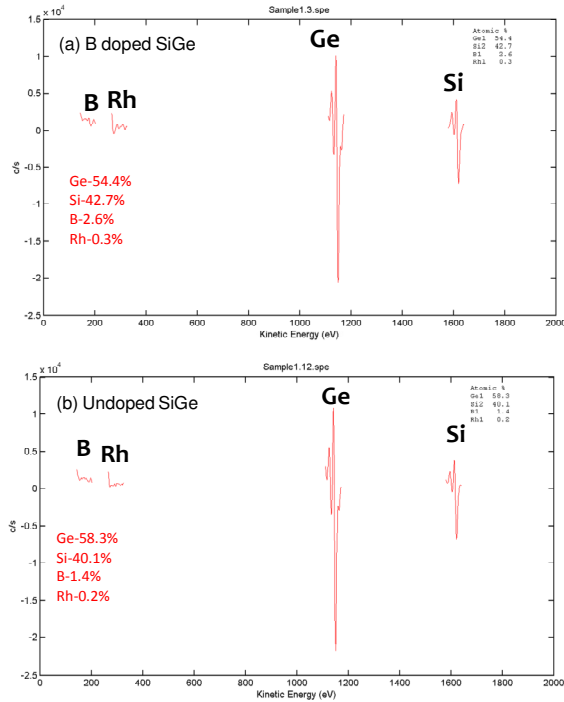

Figure 4: (a) Auger for doped SiGe film: Ge-54.4%, Si-42.7%, B-2.6%, Rh-0.3%. (b) Auger for undoped SiGe film: Ge-58.3%, Si-40.1%, B-1.4%, Rh-0.2%; (c) Auger for Ge film (100% Ge).
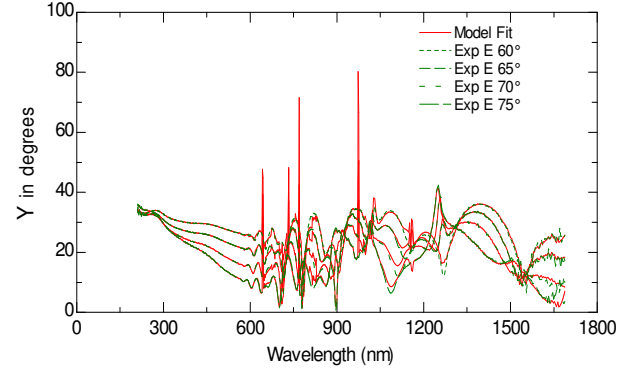

Figure 5: Woollam fit for measured data from SiGe/Oxide/Si stack. Final parameters: 115Å surface roughness, 10213Å Si$_x$Ge$_{1-x}$ where x=0.342, 15112Å thermal oxide, and 1mm Si.

Table 4: Measured sheet resistances for the B doped and undoped SiGe films.

SiGe film	Average [$\Omega/\square$]	Max [$\Omega/\square$]	Min [$\Omega/\square$]	Variation
450^{0}C SiH$_4$/GeH$_4$/B$_2$H$_6$: 100/50/20	20.24	29.17	14.80	29.45%
400^{0}C SiH$_4$/GeH$_4$/B$_2$H$_6$: 100/50/20	19.92	16.17	24.24	20.64%
400^{0}C SiH$_4$/GeH$_4$/B$_2$H$_6$: 100/50/0 (no doping)	6.81×10^5	2.17×10^5	1.24×10^6	78.3%

3.4 Stress Measurement

The stress was measured on 1µm thick films using the stresstest tool. The test was done by measuring the initial curvature of the wafer with 1.5µm thick LTO on both sides. The film was deposited with the parameters listed in Table 5. The film on the back side of the wafer was etched using recipe 1 in Lampoly. Wafer 1 had 200s of etching but the film appeared to be fully etched after 100s of the main etch step according to the endpoint detection. This corresponds to an etch rate of 6000Å /min which is nearly double the etch rate of polysilicon. Wafers

2, 3, and 4 were etched for 110s. This affected the stress measurement for wafer 1 compared to wafers 2, 3, and 4. The average stress for wafers 2, 3, and 4 is 94MPa (compressive).

Table 5: stress measurement for 1um film under 400mTorr, 450^0C, SiH_4-100sccm, GeH_4-50sccm, B_2H_6-20sccm, 2-hour deposition.

	Stress
Wafer 1	45MPa (Compressive)
Wafer 2	96MPa (Compressive)
Wafer 3	99MPa (Compressive)
Wafer 4	87MPa (Compressive)

3.5 Released Cantilever Structure

As discussed in section 3.4, our low-temperature SiGe films showed low stress. To confirm the stress measurement, we patterned a variety of test structures including arrays of cantilever beams, fixed-fixed beams, Guckel rings, and other stress measurement structures. Additionally, we also fabricated NEM relays as well to see if it is possible to build micro/nanoscale mechanical structures with this film.
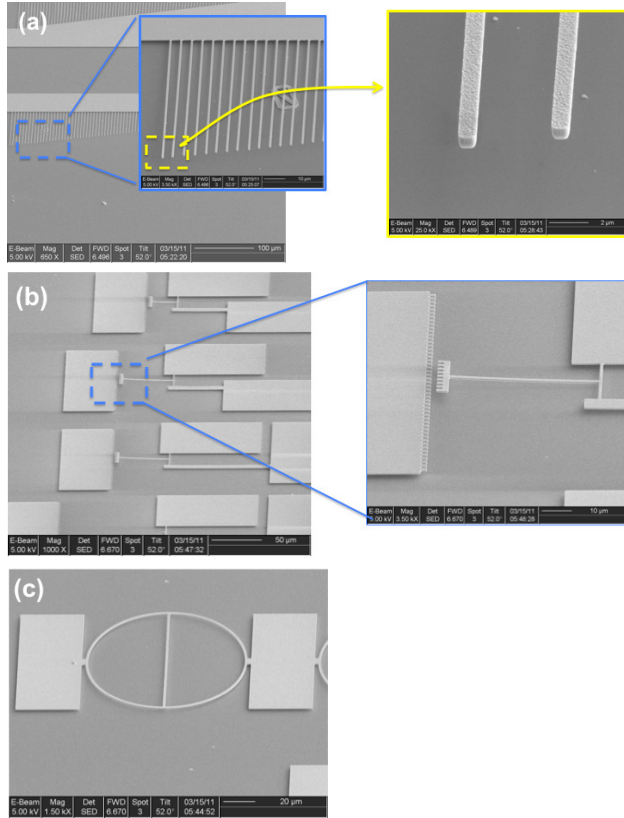

Figure 6: SEM images of three types of micro-mechanical structures using SiGe film: (a) series of cantilever beams; (b) strain gauge structures; (c) Guckel rings.

We patterned our SiGe film using 0.7µm 955 resist and photolithography (ASML tool), and etched the SiGe using recipe 1 in Lampoly with the main etch time set at 110s. The patterned wafers were then etched in HF to remove the SiO_2 beneath the

patterned structures. Then, we released the device using critical point dry (CPD tool).

Figure 6 a, b and c show three types mechanical structures we fabricated: Fig. 6a is a series of cantilever beams; Fig. 6b shows SiGe strain gauge test structures; Fig. 6c are Guckel rings structures. As seen in Figure 6, none of these mechanical structures showed significant buckling or curving up, indicating low stress inside the SiGe film.
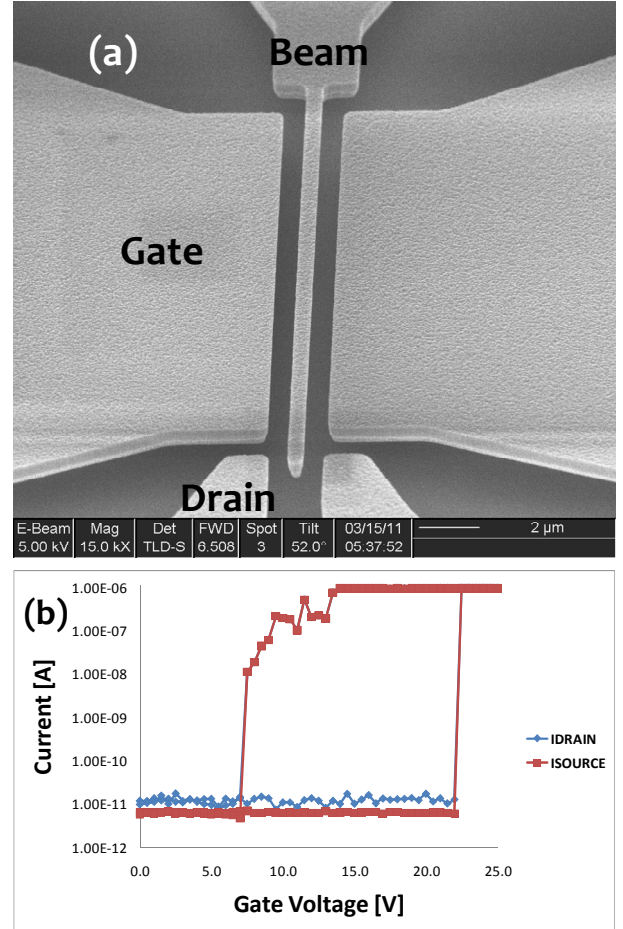

Figure 7: Fabricated nanoelectromechanical (NEM) relay using the low-temperature SiGe film (a) SEM of fabricated device. (b) I-V characteristics of the NEM relay confirming the correct functionality (V_{DRAIN}=2.35V, V_{SOURCE}=0V).

As shown in Section 3.4, effective B doping for SiGe film has been confirmed through sheet resistance measurements. Low sheet resistance enabled us to build nanoelectromechanical (NEM) relays using these low-stress SiGe films Figure 7 shows an SEM of one of the fabricated NEM relays with the deposited SiGe as the structural material. To actuate the relay, we applied 0V to the beam, and swept the gate voltage. Due to the electrostatic force between the beam and gate, the beam is attracted toward the gate. However, the SiGe beam has elastic force to resist the electrostatic force exerted by the gate electrode. When increasing V_{GS} to a certain value (defined as pull-in voltage), the beam pulls in toward the gate connecting the beam and drain. Since we applied 2.35V to the drain electrode, we observed current flowing from drain to

the gate. When V_{GS} is reduced from the pull-in voltage to a certain value (defined as pull-out voltage), the beam is released from the gate, disconnecting the beam from the drain. As can be seen from the I-V characteristics of the fabricated SiGe NEM relay, our low temperature SiGe film is a good candidate material for NEM relay structural material. In order to get good NEM relay, the beam material needs to have not only good mechanical properties, but also good electrical conductivity. In practice, the sidewalls are coated with a hard conductive material to improve current flow.

4   Discussion
4.1 Sheet resistance

For each wafer, we measured five points across each wafer. Table 4 shows a summary of the measured results.

As seen from the Table 4, the average sheet resistances of the doped SiGe film are much smaller than the undoped one. Moreover, the variations of sheet resistance across the doped SiGe film are less than 30%, which are probably due to the thickness variations across the whole wafer. However, the sheet resistance variation of the undoped SiGe film is much larger (78.3%). Since there is no active dopant in the undoped SiGe film, the poor conductivity of the undoped SiGe film may due to the grain boundary of the undoped poly-crystalline SiGe film, which may have large variation. Hence, the measured larger variation in the sheet resistance in the undoped SiGe film is consistent with our expectation.

4.2 Stress Measurement

As discussed in Sec. 3.4, we measured the stress for four wafers with SiGe films 1um film deposited under 400mTorr, 450^0C, SiH_4-100sccm, GeH_4-50sccm, B_2H_6-20sccm. Due to the backside oxide etching, wafer #1 the stress of wafer #1 was quite different than the other three wafers. Wafer to wafer variation obtained from wafer #2, 3, and 4 is 5.1%. A better way to characterize the stress and stress gradient is to further analyze the patterned stress test structures.

4.3 XPS and Auger Measurements

The XPS data for the SiGe film showed approximately the Ge to Si ratio expected. However, there were a number of unexpected contaminants in the film. First, there was P even though we doped it with B. Second, Rh is not used in the lab and is a very expensive metal. Third, Na would be especially bad for a clean tube in SNF. Last, the O contamination was much worse than expected. The Ge film had similar problems. Due to the discrepancy between our expectations and the XPS measurement results, we took Auger measurements, which are shown in Figure 4a, b, and c. These measurements were also done after sputtering. The Auger results were more in line with our expectations. The

Ge to Si ratio was slightly less than expected. However, there was some B in the sample and no Rh, C, or O detected. The undoped SiGe film had slightly less B in the film although with this resolution of scan it is unknown if these levels are below the noise floor of the detector (1.4% compared to 2.6%). The Ge film matched the textbook example for the Auger response to Ge without any other elements present. The XPS measurements could be repeated using the charge neutralization gun to correct for oxide charging. Another potential solution would be to deposit the film directly on Si wafers.

5   Conclusion

Our initial goal was to develop a low stress (<50MPa), 1µm SiGe film that can be deposited at CMOS compatible temperatures ($\leq 450^0$C) with a composition of approximately $Si_{0.35}Ge_{0.65}$. We successfully demonstrated 1µm thick SiGe films with stress less than 100MPa and deposition temperatures of 400^0C. We also found that SiGe films do not require a Si seed layer and can be directly deposited on low temperature oxide layers. This significantly simplifies the deposition process. Future directions for this project include exploring the film composition with different precursor gas flows and developing a good method to more accurately measure the thickness using ellipsometry.

6   ACKNOWLEDGMENTS

7   REFERENCES

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