# EE410 CMOS Process Documents

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## SECTION 1 - Runsheet Revisions

This process has been developed with the help of many people, most without attribution. This section is intended to set that straight, and keep a log of changes*. As things are changed, add them to this list!*

- This process was developed by Alvin Loke in ’94, with some parts based on an earlier process.
- Field oxide etch modified from dry etch to wet. This provides better step control and avoids plasma damage to active silicon.
- 1998 Vivek Subramanian, Celisa Date: Metal thickness increased from 0.5 to 1.0 microns for better step coverage. Resist hardening for n+ select reduced to ease strip.
- 1999 Aaron Partridge, with input from Jitendra Mohan, Ken Honer and Bart Kane: Deep well implant energy reduced from 200KeV to 180keV because the implanter is not reliable at 200KeV. Gate oxide regrown just prior to poly deposition for clean gates. Gate reoxidation concatenated with poly dep to minimize gate exposure. Poly etch changed from isotropic to vertical because stringers are not a problem with wet FOX etch, and steep sidewalls improve gate length control. Resist hardening bake on n+ select reduced form 180C to 110C to avoid reticulation. LTO deposition and reflow concatenated to avoid reentrant steps. This document expanded in various descriptions.
- 2000, 2001 Aaron Partridge, Pranav Kalavade: N++ implant dropped from 180KeV to 100KeV for easier outside implants. N++ drive added to push arsenic. Resist spin and development updated to new resist and programs. Resist descum added prior to active etch for good wetting. Resist stripper updated. LTO drive switched from inner to wet. Other small updates.
- 2002 Nabeel Ibrahim, Steve Jurichich, and Jim McVittie: Al/Si Etch changed from Wet to Dry Etch. Schedule modified (by Chi On Chui and Nabeel Ibrahim) to distribute processing more evenly throughout the quarter. Additional cleans and postbakes added as necessary because of modified schedule. Change N++ implant back to 180KeV from 100KeV as implants will be done in-house, drop drive-in step.
- 2003 Chi On Chui, Rohit Shoney: New Ultratech reticles (EE410A_03 & EE410B_03) made with new Vernier mark sets added. The PAD level removed. Two new fields added for contact metal liftoff (METAL_LO) and SOI/LOCOS isolation (ACTIVE_R), respectively. N++ implant dropped again from 180KeV to ??KeV for easier outside implants. N++ drive-in revoked to push arsenic. Both the runsheet and instruction manual updated.
- 2006 Dawson Wong: Replaced Standard, Matrix, and PRX-127 resist strips with Gasonics. Deleted silicon etch after contact hole etch. Deleted plasma freckle etch after metal etch. Furnaces use N2 ambient instead of Ar. Increased resist thickness for Photolithography #6 to 1.6 um. Updated conditions for implants, poly etch and contact hole etch. Updated Tylan tube numbers.
- 2007 SNF Process Staff: Transferred from Ultratech stepper to ASML. Transferred to "Clean" equipment. Defined "Standard" cleans. Updated process descriptions in this document. Developed EE410 industry-style runcard that travels with the wafers as they are processed.

# SECTION 2 - Best Known Fab Practices

## 2A. Plan your process flow BEFORE you begin

As best as you can, create a detailed runsheet. Include the appropriate equipment selection, making sure that the "Clean", "Semiclean" and "Gold-Contaminated" requirements are met. Make sure that all the appropriate clean and resist strip modules are in place (for example, a typical newbie mistake is to specify piranha cleaning of wafers with metal on them.) Make sure to include as much detail as possible, including where you should perform inspections and measurements. It's best to start out with a well-established runsheet and build your process flow from that. Even if you are an experienced labmember, it's also highly recommended that you have another experienced labmate help review your process flow beforehand. And please feel free to consult with your favorite SNF Process Staff person – this is why they are here!

## 2B. Inspect, inspect, INSPECT!!

It is absolutely critical that you inspect your wafers at each step in the process, particularly in a fully integrated, multimodule process flow such as required for the EE410 device. Why? Because process problems WILL happen; equipment problems WILL happen. It is rare, even in the best industrial organizations, for a new device/new process to be executed the first time without a glitch. However, the likelihood that you'll be able to rework and rescue your devices is significantly better if you catch the problem immediately; one or two steps later, it may be impossible to rework the wafers and you might have to start from scratch again. Given the weeks of lab time you will invest in each of your device wafer runs, think of frequent inspections as added insurance against having to start over.

**2B.1. INSPECTIONS –** There are three general types of inspections:

**Whole Wafer Visual Inspection:**

- Whenever handling wafers, such as when loading and unloading from furnaces or other equipment, or manually transferring wafers from one boat or cassette to another, or selecting sample wafers for other inspections or measurements, you should do a visual inspection of the whole wafer.
- Check for gross defects, such as particles and scratches. Many gross defects are systematic (i.e., scratches in the same place on every wafer; particles only on the wafer edges, etc.) and most are pretty random (i.e., one scratch on one wafer.) Make sure to note your observations.
- Check for color and color uniformity. Semitransparent films will exhibit dramatic color changes with relatively small variations in color. Wrong color or inconsistency in color are easy to see.
- Make sure to check wafer backsides as well! Defects on the backside can create problems on some equipment and may result in mis-processed wafers.
- A variation: whole-wafer inspection under UV-light is helpful for finding surface asperities, such as particles, scratches, or resist spin defects. A low power, green-light UV inspection lamp can be found in the lithography area, near the SVG coat tracks.

**Microscope Inspection**:

- Select a few wafers from each batch processed for inspection under the microscope. You should inspect enough wafers to make YOU feel reasonably confident that the batch of wafers

have been processed successfully. Admittedly, this is a matter of experience and some personal judgment about the reliability of a specific process step and the risk you are willing to take of possibly losing a wafer to misprocessing for one reason or another. But a general recommendation is to perform microscope inspection on 20%-25% wafers in the batch; though certainly, inspecting all of them is also recommended, especially if you have only a few wafers to begin with.

- Before putting the wafer under the microscope, take a moment to perform a visual inspection of the whole wafer.
- Microscope inspection should be done in several spots across the wafer. A typical inspection would consist of an X-scan and Y-scan across the wafer, stopping at several random points, followed by area inspections at five specific points on the wafer (top, center, bottom, left, and right.) It is easiest to inspect the same die area in each of these locations, in order to make the best comparison. The area inspected should include the most critical features being defined at that particular process step (i.e., inspection for an etch would include checking for residual film, resolution, and undercutting, as appropriate.)

**Film Thickness Measurement:**

- Thickness measurements are typically done after oxidation or film deposition to ensure the appropriate film thickness is achieved. Depending on the etch, they are also done after etching to ensure the etch is complete and/or the film is completely removed.
- As in the microscope inspection, select a sampling of wafers that assures YOU that the wafers have been processed appropriately.
- Before putting the wafer under the microscope, take a moment to perform a visual inspection of the whole wafer.
- Thickness measurements are typically done at several points across each wafer (top, center, bottom, left, and right.) Measurements may be done on blank test wafers (for example, base silicon dummy wafers which have been processed in a deposition furnace with your device wafers). Measurements can also be done in specific die locations which have the appropriate exposed film areas. Or both. Make sure to note your observations on the runsheet.
- For the EE410 device, the measurement locations are indicated:
  - Four sets of fabrication test structures, located at the corners of each die (excluding the SEM structures), are provided for consistent measurement of oxide and poly thicknesses.
  - After definition of the active region, the fabrication test structures will be patterned on the wafers. Select any one of the 4 corners for oxide and poly measurements. Be consistent with which corner was selected.

## 2B.2. WHEN TO INSPECT – The best places to inspect are as follows:

**After photopatterning wafers:**

- Microscope inspection of sample wafers for pattern resolution and alignment
- Visual inspection for gross defects and to ensure patterning on all wafers.
- Rework resist by stripping resist and repatterning as necessary.

**After oxidation or thin film deposition:**

- Thickness/uniformity measurement of sample wafers by Nanospec or profilometry, as appropriate

- Visual inspection for gross defects, surface quality, and color (for semi-transparent films).
- Rework is possible, depending on the problem.

**After etching:**

- Microscope inspection of sample wafers for pattern resolution and etch quality.
- Thickness/uniformity measurement of sample wafers by Nanospec or profilometry, as appropriate
- Visual inspection for gross defects, surface quality, and color.
- Rework or re-etch may be possible, depending on the problem.

**After resist stripping:**

- Microscope inspection of sample wafers to ensure resist removal. Check also for pattern resolution and etch quality.
- Thickness/uniformity measurement of sample wafers by Nanospec or profilometry, as appropriate.
- Visual inspection for residual resist, gross defects, surface quality, and color.
- Rework may be possible, depending on the problem.

**Whenever handling wafers:**

- Such as upon manual loading and unloading from furnaces or on transferring to different wafer boats or cassettes:
- Visual inspection for residual resist, gross defects, surface quality, and color.
- Rework may be possible, depending on the problem.

## 2C. Record Your Observations!!

This simply cannot be emphasized enough. If there are problems, or if the run works and you want to recreate it exactly, it is absolutely important to have good notes. While this is true in general for lab work, it is doubly true in the clean room, since we have so many hundreds of variables to control.

- Make sure that you record any important processing details and/or problems that you observe on the run sheets. A good record of important observations will become extremely important especially when you are trying to account for anomalies in subsequent processing and in wafer testing.
- Information worth recording: the specific equipment used, the date and time the wafers were processed on the equipment, who did the processing (if not you), any general observations (such as wafer color or other appearance), processing problems (i.e., any equipment warning noted, whether you think it directly affects your process at the time or not), any rework done, any anomolies observed on specific wafers (making sure to include wafer ID's.) Remember: the smallest detail may be an important clue later!
- It is a good idea to sketch wafer cross-sectional and top-view diagrams after various processing steps. This exercise will undoubtedly better your understanding of what is happening to the wafers.
- Make sure to keep your notes in a traceable, organized fashion -- remember. Use your lab notebook and/or a detailed runsheet. Common newbie mistake: relying on notes taken on lab wipes!

# SECTION 3 - Process Modules

## 3A. Wafer Cleaning & Resist Stripping:

Proper wafer cleaning is essential, not only for your own process, but for everyone else sharing the equipment. It is essential that everyone abide by the cleaning protocols to ensure against contamination and cross-contamination. The clean procedures at SNF are based on procedures commonly used semiconductor cleanroom from the mid-1980's. Since then, modern electronics production fabs have eliminated many cleans in order to reduce wafer handling and water consumption, as die yield and production costs are paramount. However, in research labs, such as ours, flexibility to accomodate a wide variety of processes and materials is paramount. Thus, SNF relies heavily on wet cleans to allow broader process margins and guard against cross-contamination.

- Always put a second pair of vinyl gloves over your first pair before handling any wafer cassettes. Be particularly careful to put on a clean pair of vinyl gloves when handling the cassette before and after the spin dry. THIS IS VERY VERY IMPORTANT.
- The acid hot pots the wet benches are rather deep. When inserting and removing cassettes from the acid bath, it is best to put on an acid-resistant glove over your flexiglove and then another flexiglove over the acid-resistant glove in order to protect your hand when grabbing the cassette handle. Also, leave the cassette handle in place when immersing the cassettes in the acid bath or placing them in the dump rinser.
- Bubbling acid can cause wafers to float out of the cassette in the sulfuric hot pot. Always watch your cassette for signs of severe bubbling on the resist, and agitate as necessary.

### 3A. 1. Standard Piranha Clean: *wbnonmetal*

**Purpose:** To remove trace organics, including non-hardened photoresist.

**Method:** "Piranha" is a heated mixture of concentrated sulfuric acid, hydrogen peroxide and water. The sulfuric acid oxidizes organic materials. The peroxide provides the source of oxygen, yielding $CO_2$ and water as byproducts. Old or heavily-used piranha mixture isn't as effective; additional peroxide can restore the activity. Piranha clean is an easy-to-use method with a very broad processing window. It does, however, mildly oxidize silicon surfaces. Piranha will corrode non-noble metals. At ***wbnonmetal***, labmembers pour a mixture of 9 parts concentrated sulfuric acid (about 98% pure acid) to 1 part of hydrogen peroxide (30% in water) into hot pots which are temperature controlled to 120 C.

**When to use:** "Clean" class wafers (no metals) which may have organic residues or non-hardened resist on them. New wafers straight from the storage box should be piranha cleaned before use (although "prime" wafers go into the storage boxes at the packaging facilities CMOS clean, plasticizers from the storage boxes will outgas onto the wafers). Wafers with photoresist can be piranha-cleaned, provided the resist has not been plasma- or bake- "hardened." Wafers with "hardened" or thick resist (3 microns or greater) should be first plasma cleaned in the ***gasonics*** and then cleaned in piranha.

**Procedure:**

- At ***wbnonmetal***, dip for 20 minutes in 9:1 concentrated sulfuric acid: 30% hydrogen peroxide, heated to 120 C
- Rinse in the quick dump rinse tank for 6 cycles (about 4 minutes)
- Spin rinse/dry in the Semitool spinner (about 5 minutes)
- Visually inspect to ensure complete resist removal

## 3A. 2. Standard Hard Resist Strip: *gasonics* and *wbnonmetal*

**Purpose:** To remove hardened photoresist from "clean" wafers.

**Method:** As described above, certain processes (including longer plasma etches, heavy ion implantations, hard bakes or UV cures) can cross-link the resist surface, leaving a hardened "skin" which can be removed using oxygen plasma. The ***gasonics*** plasma etcher is recommended for removing resist from "Clean" substrates. The ***gasonics*** is a downstream, microwave plasma system which uses quartz lamps to heat the substrate for more efficient resist removal. "Downstream" is critical for CMOS; in the ***matrix*** and in other plasma etchers in the lab, the substrate resides directly between the RF electrodes generating the plasma. This leads to plasma damage if the silicon gate is exposed; this also leads to device damage due to the "antenna effect" when metal lines are exposed. Since the oxygen plasma in the ***gasonics*** is generated upstream of the substrate, such damage is avoided in this system. (So, when designing your CMOS process flows, make sure to be careful in your selection of available equiment!) Processing on the ***gasonics*** alone can leave some residual organic particulate on the wafer edge. So, a short, piranha clean following plasma strip is done.

**When to use:** For "clean" wafers in which resist may have been hardened. Also recommended for "clean" wafers with thick photoresist, hardened or not.

**How to process:**

- Process in ***gasonics***, program 013.
- Shortened piranha clean at ***wbnonmetal***: 10 minutes in 9:1 concentrated sulfuric acid & 30% hydrogen peroxide, heated to 120 C
- Rinse in the quick dump rinse tank for 6 cycles (about 4 minutes)
- Spin rinse/dry in the Semitool spinner (about 5 minutes)
- Visually inspect to ensure complete resist removal

## 3A. 3. Standard Metal Layer Resist Strip: *gasonics* and *wbmetal*

**Purpose:** To remove photoresist from "semiclean" wafers.

**Method:** Piranha corrodes non-noble metals, including aluminum. So, resist removal consists of ashing the resist in the ***gasonics*** etcher, followed by dipping in PRX-1000, a commercial, alkaline-based organics stripper. The PRX-1000 dip is also used as the standard pre-anneal

clean, to remove any residual plasticizers or other contaminants which may adhere to wafers which have been sitting around for a while. Another variation of the standard resist strip process for metal-containing wafers may include a 10 minute PRX-127 dip between the ***gasonics*** clean and PRX-1000 dip. PRX-127 is another commercially available, alkaline-based stripper which has added selectivity for removal of the residual side-wall polymer which accumulates during plasma metal etch. It is absolutely critical that wafers be perfectly dry (especially if sequential dips are used) since trace moisture yields a highly alkaline solution which will corrode metal.

**When to use:** For resist removal from "semiclean" substrates.

**How to process:**

- Process in ***gasonics***, program 013.
- At ***wbmetal***: 10 minutes in PRX-1000 at 40 C.
- Rinse in the quick dump rinse tank for 6 cycles (about 4 minutes)
- Spin rinse/dry in the Semitool spinner (about 5 minutes)
- Visually inspect to ensure complete resist removal

## 3A. 4. Standard Pre-Diffusion Clean: *wbdiff*

**Purpose:** To decontaminate wafers before furnace processing.

**Method:** The process used at SNF is a modified "RCA" clean, originally developed at RCA in the 1960's as a way to decontaminate wafers before furnace or deposition steps. The RCA clean consists of an RC-1 mixture of ammonia, hydrogen peroxide and water; this removes particles and surface contaminants by simultaneously mildly oxidizing the silicon and dissolving the resulting oxide to undercut the contaminant. Although very effective, the process margin is narrow and can easily lead to silicon pitting and plating of metal ions. This is followed by an RC-2 mixture consisting of hydrochloric acid, hydrogen peroxide, and water, which is effective at remove trace metals. Instead of the RC-1, at SNF we use a piranha dip (which mildly oxidizes the silicon surface) followed by an HF dip (which dissolves the resulting oxide), a sequence which has a broader process window.

**When to use:** For "clean" before processing in any furnace. Wafers must be processed through piranha clean at ***wbnonmetal*** prior to pre-diffusion cleaning at ***wbdiff.***

**How to process:**

- At ***wbdiff,*** dip for 10 minutes in 4:1 concentrated sulfuric acid: 30% hydrogen peroxide at 90 C.
- Rinse in the quick dump rinse tank for 6 cycles (about 4 minutes)
- Dip for 30 second in 50:1 HF
- Rinse in the quick dump rinse tank for 6 cycles (about 4 minutes)
- Dip for 10 minutes in 5:1:1 water: concentrated hydrochloric acid: 30% hydrogen peroxide.
- Rinse in the quick dump rinse tank for 6 cycles (about 4 minutes)

- Spin rinse/dry in the Semitool spinner (about 5 minutes)

### 3A. 4. Standard Pre-Metal Deposition Clean: *wbdiff*

**Purpose:** To decontaminate wafers before metal film deposition and minimize native oxide formation.

**Method:** The process is nearly identical to the "Standard Pre-Diffusion Clean" but with the addition of another HF dip to minimize the native oxide which can form in the highly oxidizing environment of the last heated 5:1:1 bath (water: hydrochloric: peroxide). Alternatively, another acceptable method is to perform the same dips, but in modified order: piranha, hydrochloric/peroxide, the 50:1 HF. However, the first method is recommended; cycle time increases by about five minutes, but the process is more consistent with the rationale of the RCA clean than the second.

**When to use:** For "clean" before processing in any furnace. Wafers must be processed through piranha clean at ***wbnonmetal*** prior to pre-diffusion cleaning at ***wbdiff.***

#### How to process:

- At ***wbdiff,*** dip for 10 minutes in 4:1 concentrated sulfuric acid: 30% hydrogen peroxide at 90 C.
- Rinse in the quick dump rinse tank for 6 cycles (about 4 minutes)
- Dip for 30 second in 50:1 HF
- Rinse in the quick dump rinse tank for 6 cycles (about 4 minutes)
- Dip for 10 minutes in 5:1:1 water: concentrated hydrochloric acid: 30% hydrogen peroxide.
- Rinse in the quick dump rinse tank for 6 cycles (about 4 minutes)
- Dip for 30 second in 50:1 HF
- Rinse in the quick dump rinse tank for 6 cycles (about 4 minutes)
- Spin rinse/dry in the Semitool spinner (about 5 minutes)

## 3B. Photomasking Modules:

### 3B.1. Description of Process Steps

Photomasking or photolithography forms the core of device fabrication. In this EE410 device, there are six photomask layers, the processing of which are nearly identical. The basic steps of photomasking are as follows:

- **Singe/Prime: S**inge bake drives off surface moisture which interferes with coating by hexamethyldisilazane (HMDS). Hydrophillic surfaces coated with HMDS become hydrophobic, allowing better coverage and adhesion to resist.

- **Spin coat:** Photoresist, in viscous liquid form, is dispensed onto a spinning substrate. By controlling the conditions of dispensing and spin speeds, resist is applied in a uniform

coat. Additionally, solvent may dispensed on the wafer backside, in order to ensure the wafer backside is clear of resist, and on the wafer edge, to remove resist on the edge ("Edge Bead Removal" or "EBR"). Residual resist on the wafer backside can result in processing problems later on (particularly during expose). EBR is helpful in eliminating resist particulates (by removing "threads" of resist which form at the edge) and helps avoid problems in etch tools, where sticky resist can result in wafer handling problems.

- **Pre-bake:** To drive off excess solvent from the resist. Before pre-bake, wafers are considered to contain hazardous chemicals and may be handled only under exhausted areas of the lab. Once wafers undergo pre-bake, they may be handled in the breathing areas of the lab.

- **Expose:** The photoresist is patterned by exposure to UV illumination. More about this in section 4C.

- **Post-expose bake:** This is used to "set" chemically-amplified resists, such as the 3612 resist, so that finer features and more vertical-wall profiles can be achieved. This is optional – whether you need to do this depends on your process requirement – but is recommended for desired resolutions of less than 2 microns.

- **Develop:** Removes resist in UV-exposed areas (positive resists).

- **Post-develop bake:** To drive off moisture, harden the resist or reflow sharp resist profile corners. Although this is built into the EE410 process flow, for other devices, this can be considered optional, depending on your process needs.

## 3B.1. Equipment Sequence

- **Singe/Prime:** ***yes*** prime oven**.** One cycle does both singe and prime. Alternatively, singe can be accomplished by 30 minute bake in 150 C Singe oven, followed by vapor track prime on ***svgcoat/2*.** Following vapor prime in the ***yes***, wafers will remain sufficiently hydrophobic for several days for spin coating with resist.

- **Spin coat/Pre-bake:** ***svgcoat/2*.** The spin station allows you to prime, apply any of the standard resists, and pre-bake using several pre-programmed recipes.

  For the first five photomasks in the EE410 device, one micron of 3612 resist will be applied, using programs:
  - 9 (to skip track prime, since this is done in the ***yes***),
  - 7 (to dispense 1.0 μm of Shipley 3612 resist), and
  - 1 (to pre-bake 1.0 μm resist appropriately.)

  For the last, metal photomask, thicker resist is applied, using programs
  - 9 (to skip track prime, since this is done in the ***yes***),
  - **8** (to dispense **1.6** μm of Shipley 3612 resist), and

- **2** (to pre-bake thicker resist appropriately.)

- **Expose:** ***asml.*** The photoresist is patterned by exposure to UV illumination. More about this in section 4C.

- **Post-expose Bake:** ***svgdev/2.*** The hot plate on the spin track can be used for post-expose bake:

  For the first five photomasks in the EE410 device, which have one micron of 3612 resist, use programs:
  - 9 (to skip developer dispense),
  - 1 (for post-expose bake of 1.0 μm resist.)

  For the last, metal photomask, which has thicker resist, use programs
  - 9 (to skip developer dispense),
  - **2** (for post-expose bake of **1.6** μm resist.)

- **Develop/Post-Develop Bake:** ***svgdev/2*** is a two-track systems with standard developer recipes preprogrammed.

  For the first five photomasks in the EE410 device, which have one micron of 3612 resist, use programs:
  - 8 (develop for 1.0 μm resist),
  - 1 (for post-develop bake of 1.0 μm resist.)

  For the last, metal photomask, which has thicker resist, use programs
  - 4 (develop for 1.6 μm resist),
  - **2** (for post-develop bake of 1.6 μm resist.)

- **Additional Post-Develop Bake:** Although this is done in-line on the ***svgdev/2*** tracks, this can also be done in the standard 100 C oven (30 minutes). This is done in the EE10 process flow whenever wafers with resist have sat for a period of time following photomasking.

## 3C. ASML PAS 5500/60 Stepper System

For 2008, EE410 will be photopatterned on the ASML PAS 5500/60 system recently installed at SNF. This is a 5:1 reducing I-line stepper, capable of resolution down to 0.35 microns. Rather than the field-to-field alignment scheme of the Ultratech stepper used in previous years, the ASML, instead, uses wafer-level alignment marks which are laid down in the silicon substrate "zero layer" photomask. Although this requires an additional masking layer, the process is simple and yields a remarkably robust and flexible alignment scheme. For more detail on the ASML system, see the operations manual posted on the SNF website.

For EE410, there are three reticle masks, each with two images, for a total of six images, one for each photomask layer (the "zero layer" is patterned using "PM" marks available on a standard ASML-

provided reticle.) No changes were made to the layout, which was derived from a GDS file dating from August 2005, except to rotate the die by 90 degrees. The die dimensions are:

Wafer level: X = 8 mm Y = 16 mm.
Mask level: X = 40 mm Y = 60 mm.

Remember, the mask level is 5-fold larger than the projected pattern at the wafer level. The two images/layers on each mask reticle are separated by a solid band of chrome, 6 mm wide in the X-direction (mask level.) Thus, the offsets for the center of the images versus the center of the mask reticle are: X = +/- 23 mm and Y = 0 mm.

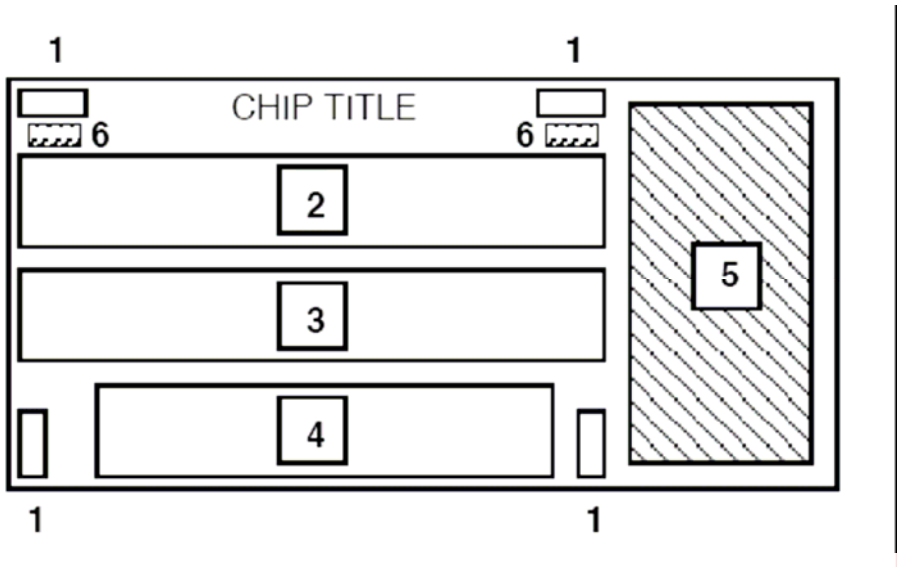
The images/layers map to the mask reticle and job names as follows:

| Layer | ZERO LAYER | ACTIVE | PWELL | POLY | NSELECT | CONTACT | METAL |
|---|---|---|---|---|---|---|---|
| Job Name | EE410R_1 | EE410R_1 | EE410R_1 | EE410R_1 | EE410R_1 | EE410R_1 | EE410R_1 |
| Layer ID | 0 | 1 | 2 | 3 | 5 | 6 | 4 |
| Layer # | 0 | ACTIVE | PWELL | POLY | NSELECT | CONTACT | METAL |
| Image ID | PM | ACTIVE | PWELL | POLY | NSELECT | CONTACT | METAL |
| Reticle ID | 45023981A009 | EE410RET1 | EE410RET1 | EE410RET2 | EE410RET3 | EE410RET3 | EE410RET2 |

### 3D. EE410 Device Test Structure Layout

Alvin Loke designed a set of test structures for ee410. There is more here than we have time to test, but if something goes wrong there is enough to find the problem.

- On each die, six groups of test structures will be fabricated:
  1. **F**abrication test structures (F series),
  2. **P**rocess test structures (P series),
  3. **D**evice test structures (D series),
  4. **C**ircuit test structures (C series),
  5. **SEM** test structures, and
  6. **Vernier** alignment test structures.
- These test structures are approximately fabricated in the following arrangement.



# SECTION 4 - Process Details

## 4A. Week #1: Preparation

### 1. Wafer Start (STEP 00.00):

C Prime Stock: CZ, <100> oriented, N-type (phosphorus-doped), 5 - 10 Ω-cm. Dimensions: 100 mm (4-inch) diameter, 525 ± 15 μm thickness

**Wafer Selection & Sheet Resistivity Measurement:**

Do you trust the label on the box? You shouldn't. Check at least one wafer from each box. Also, take a look to be sure the rest are in good shape and not "test" wafers.

- Measure and record the sheet resistivity of the wafers using the Tencor Instrument Sonogage. It is sufficient to do this only on test wafers.

**STANDARD PIRANHA CLEAN:**

It might seem strange, but new wafers are not very clean. In addition we have just covered them with silicon dust. So they get a full scrub down using a Standard Piranha Clean.

### 2. PM #0: Zero Level Marks (STEPS 0.100-0.190):

The ASML stepper files are setup so that all the mask layers are aligned relative to the zero level marks defined before "real device processing" begins. When setting up the run files, the user can choose one or more standard "PM" marks to be placed anywhere on the wafer at the zero layer. Ideally, these would be placed at wafer edges, although they may also be placed in scribe lines as needed. After lithography, the PM marks will be etched into the silicon substrate to a targeted depth of 1200 A, which should provide sufficient contrast for alignment. Similar PM marks are written into the reticle frame. During alignment, a laser is directed through the reticle PM mark to the wafer level PM mark. These PM marks are cleverly designed to exhibit characteristic interference patterns when wafer-level and reticle-level marks are superimposed, i.e., perfectly aligned. Thus, it is absolutely important to know exactly where your device image is relative to the reticle center. Nearly all the file definition can be done on the ASML system emulator, located outside the lab.

The litho process steps are:

- Singe & Prime in the ***yes***
- Spin coat using ***svgcoat/2*** programs 9 (no prime), 7 (1.0 μm of 3612 resist w/2 mm EBR), and 1 (prebake 90 C for 60").
- Expose on the ***asml***
  Job name: EE410R_1
  Layer ID: 0
  Layer Number: 0
  Image ID: PM
  Reticle ID 45023981A009
- Post-exposure bake on ***svgdev/2*** using programs 9 (no develop) and 1 (postexpose bake@110º C for 60").
- Resist develop on ***svgdev*** using programs 3 (develop) and 1 (postbake@110º C for 60")
- Inspect and rework as necessary.

## 3. Zero Level Silicon Etch (STEPS 0.200-0.240)

### Wafer Scribing:

Wafers should be scribed so that individual wafers can be identified, This is particularly important when wafers receive different processing, either deliberately (such as in a run "split") or through accident. The traditional method is to use a diamond scribe to scratch in the lettering either at the flat on the wafer front side or on the wafer backside. The act of scribing, however, can create weak spots which may lead to breakage as the wafer becomes stressed (with temperature cycling and/or wafer handling). Care must be taken to angle the lettering so that no lines are drawn perpendicular or parallel to the flat (in the directions of the crystal planes) and to make sure that no lines go to the edge of the wafer (edge defects tend to make wafers especially vulnerable to breakage.) The art of scribing is particularly important if scribing on base silicon wafers. Here, we are scribing just into the resist, so that the features will be patterned into the substrate as the zero level mask is processed. Wafers are numbered in order. Select two which will be used as test wafers T1 and T2.

### Silicon Etch:

Zero level PM marks can be etched using the p5000etch, the lampoly, the amtetcher and even the drytek2. For the sake of tradition, we used the amtetcher here, although labmembers have used the other tools as well. Following etch, the Standard Hard Resist Strip is used.

## 4. Blanket Implant (STEPS 0.300-0.340):

Ion implants are performed by outside commercial services. There are several in the Bay Area which provide a broad range of capability and fast turnaround. Ion implantation is now regarded as a commodity service -- even larger semiconductor organizations prefer to rely on outside services. For this blanket implant:

Species: Phosphorus
Energy: 100 KeV
Dose: $1.75 \cdot 10^{12}$ cm$^{-2}$
Beam Current: no limit
Implant Angle: 7°

Standard prediffusion clean is performed before implant.

## 5. Field Oxidation (STEPS 0.360-0.360):

The fields in most standard CMOS are LOCOS grown around patterned nitride. In this process we grow a uniform field and etch the oxide. This saves a great deal of time, but still gives good results.

- Wafer require Standard Pre-Diffusion Clean.
- Use tube ***tylan1*** or ***tylan2***.
- Program "FIELDOX" in Tylan.
- Like most furnace operations in the lab, this furnace recipe does a number of things in addition to the actual oxidation:
    - After loading the wafers in the quartz boats, the wafers are slowly inserted into the furnace at a low temperature of about 800°C. The automatic loading assembly is a

cantilever design so that the quartz boat does not slide along the surface of the quartz tube which can produce quartz dust particles. The slow insertion at a low furnace temperature is designed to prevent thermally induced slip.

- Next, the wafers are ramped from 800°C to the actual process temperature to be used in this step, which is 1000°C. This is done in a "mostly inert" ambient produced by flowing 2.4 L/min of $N_2$ and 0.1 L/min of $O_2$. A minimal amount of oxidation occurs during this step to protect the surface of the wafer. This ramp up requires about 35 min.
- The main oxidation occurs during a 10 min exposure to pure $O_2$, followed by 100 min exposure to "steam" which is produced by directly mixing 1.0 L/min of $O_2$ with 1.5 L/min of $H_2$. Safety dictates that we run a bit of excess $O_2$ so we don't actually end up with a 100% partial pressure of steam. The final step is a 10 min exposure to pure $O_2$. The bulk of the oxide thickness is produced by the steam oxidation and the short dry $O_2$ cycles on each end are used primarily to ensure stable furnace conditions prior to and after injecting the steam.
- Finally, the furnace temperature is ramped back down to about 800°C in an $N_2$ ambient prior to an automatic slow pull.

- This process takes ~3 hrs and 30 min of furnace time.
- The target field oxide thickness is ~500 nm.

## *4B. Week #1: Lab Section*

### 6. PM #1: Active Area (STEPS 1.000-1.190)

#### Field Oxide Thickness Measurement (STEP 0.380)

We can measure some layers by looking at the spectra of reflected light. This works for transparent materials like oxide and nitride, and some thin opaque layers, like poly.

- Measure the field oxide thickness on T using the Nano-spec, the thick oxide program, and the 10X objective.
- Measure 5 points on the wafer (flat down, toward you) and record the results below and on the runsheet:

Top_____

Left _____ Center _____ Right _____

Bottom _____

- You may see the four tiny PM marks a few mm from the wafer edge.

#### Active Area Lithography:

The following procedure describes the standard method for choosing the optimal stepper exposure settings on the Ultratech by running an "FEM" test (Focus Exposure Matrix.) In short, the device is patterned on the wafer in such a way that the focus is varied in one axis and the exposure energy is varied in the other. By inspecting under a microscope, you should be able to determine the optimal conditions, which can be dependent on the device pattern (amount of open

area, resolution required), and the substrate (reflectivity, film quality, patterns). In general, the 3612 resist has a broad process window, relative to the feature size in the EE410 device.

- Use T1 for a focus/exposure matrix (FEM). To get a proper feel for overand under-exposure, it is useful to run a fairly broad exposure range on the test wafer.
- Note: An exposure in the range of 60-90 mJ/cm2 on the ***asml*** is probably reasonable. Unless you are really trying to expose very small features, it is usually best to over-expose the wafers a bit. It is frustrating to realize that one or two of the wafers have scumming and need to be stripped, re-coated with resist, etc.
- Determine the proper exposure level by inspecting the test wafer under the microscope. At the lower exposure levels, you will see evidence of resist remaining in open field regions, which needs to be avoided. Even when you think that there is no "scumming" of this type, there can be residual resist in some areas. Scumming should be mostly gone by using an exposure setting of 60-90 mJ/cm2. If the process is marginal, normal wafer-to-wafer variation which may yield slightly different oxide thickness or slightly different resist thickness might result in scumming on another wafer, even at the same machine settings. At the highest levels of exposure, you should begin to see evidence of rounded features particularly if you look at the Vernier structures that contain two rectangles that are just touching at adjacent corners. After exposing wafer T1, you may want to expose another wafer at your selected setting (or a narrower exposure matrix) to confirm that everything is alright.
- We often skip this step because the needed exposure is often known from experience. If in doubt, a matrix may be run, and this should be noted in your runsheets. However, wafer T is still a good test of the expected exposure.

The litho process steps are:

- Singe & Prime in the ***yes***
- Spin coat using ***svgcoat/2*** programs 9 (no prime), 7 (1.0 μm of 3612 resist w/2 mm EBR), and 1 (prebake 90 C for 60").
- Expose on the ***asml***

  Job name: EE410R_1
  Layer ID: 1
  Layer Number: ACTIVE
  Image ID: ACTIVE
  Reticle ID: EE410RET1
- Post-exposure bake on ***svgdev/2*** using programs 9 (no develop) and 1 (post-exposure bake@110º C for 60").
- Resist develop on ***svgdev*** using programs 3 (develop) and 1 (postbake@110º C for 60")
- Inspect and rework as necessary.

## 7. Active Area Etch (STEPS 1.200-1.240):

FOX etch is performed wet so that the oxide step is gentle. This helps avoid poly stringers and improves metal step coverage. The profile is not simply isotropic but is sloped because the oxide etches slightly faster at the resist boundary. Be careful with this— a change of resist or of procedure could alter the profile. This has been tested with the 3612 and 1813 resists. This etch may also vary in length from about 400 to 600 seconds, it is a good idea to use fresh BOE.

- Postbake wafers in the 110°C oven for 30 min to assure resist has predictable undercut behavior. Cool in carrier 30 min.
- Descum the resist in Drytek2 for 30 seconds. This is IMPORTANT for good etching since it makes resist hydrophilic.
- Etch wafers in fresh BOE 6:1 until backsides clear plus 10%.
    1. Set 6:1 BOE timer to 420 seconds.
    2. Start down counter, at T=415 submerge in DI.
    3. At T=400 transfer to 6:1 BOE
    4. Agitate every 20 seconds. Begin peeking at T=300 sec.
    5. Expect wafer backs to clear (hydrophobic) at T=50 sec.
    6. Add 10% (about 40 seconds) after clear.
    7. Quickly dump rinse then spin.
- Microscope examination: The etch should look slightly undercut, about 0.5 microns. The resist should be in good condition.
- Check etched areas with the Nanospec to insure that etching is complete.

## *4C. Week #2: Preparation*

### 8. Sacrificial Oxidation (STEPS 1.250-1.340)

#### Photoresist Removal:

- Use the Standard Hard Resist Strip process to remove resist.
- After the resist removal, inspect the wafers to make sure that all of the resist is gone.

#### Sacrificial Oxidation:

The Sacrificial Oxide protects the active silicon from contamination through the well implant steps. Old versions of this process used this oxide as the gate oxide; we now regrow a fresh and clean gate oxide just prior to poly deposition.

- Process wafers through Standard Pre-Diffusion Clean.
- Use ***tylan1*** or ***tylan 2***.
- Program "GATEOX" in Tylan.
- Process summary:
    - Slow push at 800°C.
    - Ramp to 900°C in 2.4 L/min $N_2$ and 0.1 L/min.$O_2$ (20 min).
    - Oxidize: dry $O_2$ (5 min), steam (12 min), dry $O_2$ (5 min).
    - Ramp down in $N_2$ (15 min).
    - Slow pull.
- The process takes ~1 hr and 30 min of furnace time.
- The target sacrificial oxide thickness is ~40 nm.

#### Field Oxide Thickness (After Sacrificial Oxidation):

The field oxide will be a bit thicker from the sacrificial oxide grown, but also thinner from a bit of HF exposure. It's a good time to check it.

- Measure the field oxide thickness on T, using the Nanospec, the thick oxide program, and the 10X objective.
- Use the region marked F-1 on the selected wafer die.
- Measure 5 points on the wafer (flat down, toward you) and record the results below and on the runsheet:

Top_____

Left _____ Center _____ Right _____

Bottom _____

**Sacrificial Oxide Thickness:**

Since we do not have a chance to measure the gate oxide thickness (because we don't want to handle it!) we measure the sacrificial oxide thickness now. This oxide is just like the gate oxide, and the thickness should be quite similar.

- Measure the sacrificial oxide thickness on T, using the Nano-spec, the thin oxide program, and the 10X objective.
- Use the region marked F-2 on the selected wafer dies.
- Measure 5 points on the wafer (flat down, toward you) and record the results below and on the runsheet:

Top_____

Left _____ Center _____ Right _____

Bottom _____

## 9. PM #2: P-Well (STEPS 2.000-2.190)

This is the second alignment step. Note: This is a dark field mask (i.e., one that is mostly opaque) which tends to be more difficult to align than a clear field mask.

The litho process steps are:

- Singe & Prime in the ***yes***
- Spin coat using ***svgcoat/2*** programs 9 (no prime), 7 (1.0 μm of 3612 resist w/2 mm EBR), and 1 (prebake 90 C for 60").
- Expose on the ***asml***

  Job name: EE410R_1
  Layer ID: 2
  Layer Number: PWELL
  Image ID: PWELL
  Reticle ID: EE410RET1

- Post-exposure bake on ***svgdev/2*** using programs 9 (no develop) and 1 (post-expose bake@110º C for 60").
- Resist develop on ***svgdev*** using programs 3 (develop) and 1 (postbake@110º C for 60")

- Inspect. Check the alignment Verniers and record the alignment offsets. You should be able to align to within 0.5 μm from the ACTIVE level.

  Vernier #21: **PWELL to ACTIVE** (offset: ____ / ____ )

- Rework as necessary.

### 10. Double-Well Implant (STEP 2.200):

1st implant (deep):
Species: Boron
Energy: 180 KeV
Dose: 5 ·10$^{12}$ cm$^{-2}$
Beam Current: < 100 μAmps
Implant Angle: 7°

2nd implant (shallow):
Species: Boron
Energy: 50 KeV
Dose: 1.4 ·10$^{12}$ cm$^{-2}$
Beam Current: < 100 μAmps
Implant Angle: 7°

## *4D. Week #2: Lab Section*

### 11. P-Well Drive-in (STEPS 2.210-2.260)

#### Photoresist Removal and Clean:

- Remove resist using Standard Hard Resist Strip process.
- Inspect to be sure that the resist has been removed.

#### P-Well Drive-in

Process wafers through Standard Pre-Diffusion Clean before P-well Drive In:

- Use ***tylan1*** or ***tylan2.***
- Program "1000AN" in Tylan. Anneal Time = 1 hr.
- Process summary:
  - Slow push at 800°C.
  - Ramp to 1000°C in $N_2$.
  - Drive-in in $N_2$ (1 hr).
  - Ramp down in $N_2$.
  - Slow pull.
- The process takes ~2 hrs and 30 min of furnace time.

## 4E. Week #3: Preparation

### 12. Gate Oxidation/Poly Deposition (STEPS 2.300-2.420)

#### Standard Pre-Diffusion Clean

Cleanliness is the big issue here: the oxide tube should have a full TLCCLEAN clean overnight before this step. The chemicals at ***wbdiff*** should all be changed. Therefore it is best to start first thing in the morning when the pots are cold and the tube is just out of its clean.

- TCA clean tube overnight before this oxidation.
- Replace chemicals, especially the 50:1 HF.
- Follow the Standard Pre-Diffusion Clean process.

#### Gate Oxidation and Poly Deposition:

These steps must be made without interruption. The object is to get a clean gate oxide down and put a protective poly on it with the minimum of handling. Gate oxidation and poly deposition must not be split.

- After cleaning, go into the fresh 50:1 HF to strip the sacrificial oxide. Include 50% overetch from backside clear. This etch should start to clear in about 8 minutes, and so should take about 12 minutes total. It is vital that the HF be clean and fresh for this etch.
- Dump, rinse and spin to go back in the oxide tube.
- Use ***tylan1*** or ***tylan2***
- Program "GATEOX" in Tylan.
- Process summary:
    - Slow push at 800°C.
    - Ramp to 900°C in 2.4 L/min $N_2$ and 0.1 L/min.$O_2$ (20 min).
    - Oxidize: dry $O_2$ (5 min), steam (12 min), dry $O_2$ (5 min).
    - Ramp down in $N_2$ (15 min).
    - Slow pull.
- The process takes ~1 hr and 30 min of furnace time.
- The target gate oxide thickness is ~40 nm.
- Prepare the poly tube to accept the wafers exactly when they pull with fresh gate oxide. The wafers should be transferred in their clean holder directly to the poly tube without shelf-time. This requires timing the poly vent with the oxide tube pull.
- Use ***tylanpoly.***
- Program "AMOR4006" in Tylan.
- The poly is deposited at a temperature lower than typical process (~620°C). The film is actually in amorphous instead of polycrystalline form.
- Process summary:
    - Slow push and pumpdown.
    - Shut off gate valve and check that the system pressure does not rise more than 60 mT in 1 min.
    - Stabilize temperature: Center = 560°C
    - Deposit poly by flowing $SiH_4$ at a pressure of 400 mT.
    - Purge and backfill to atmospheric pressure.
    - Slow pull.

- Remove the wavers and run "POLYPUMP".
- The target poly thickness is ~500 nm.
- This step takes ~3 hrs of tube time.

## 13. PM #3 Polisilicon (STEPS 3.000-3.190)

### Poly Thickness (STEP 2.420):

The Nanospec can measure semi-transparent films (thin poly), but requires the underlying oxide thickness. In this case examine the poly over the active cuts and enter the measured gate oxide thickness.

- Make sure that the Nano-spec is focused on a poly region not covered by resist.
- Measure the poly thickness on T, using the Nano-spec, the poly on oxide program, and the 10X objective.
- Use F-6 (poly on gate oxide) on the selected wafer dies.
- Measure 5 points on the wafer (flat down, toward you) and record the results below and on the runsheet:

Top_____

Left _____ Center _____ Right _____

Bottom _____

### Photomask #3 Polysilicon Lithography

This step delineates the gates. It is important that the lithography be performed with care to keep the gates the correct lengths. Also, examine that the gate/active overlap is sufficient.

The litho process steps are:

- Singe & Prime in the ***yes***
- Spin coat using ***svgcoat/2*** programs 9 (no prime), 7 (1.0 μm of 3612 resist w/2 mm EBR), and 1 (prebake 90 C for 60").
- Expose on the ***asml***

  Job name: EE410R_1
  Layer ID: 3
  Layer Number: POLY
  Image ID: POLY
  Reticle ID: EE410RET2
- Post-exposure bake on ***svgdev/2*** using programs 9 (no develop) and 1 (post-expose bake@110º C for 60").
- Resist develop on ***svgdev*** using programs 3 (develop) and 1 (postbake@110º C for 60")
- Inspect. Check the alignment Verniers and record the alignment offsets. You should be able to align to within 0.5 μm from the ACTIVE level.

  Vernier #31: **POLY to ACTIVE** (offset: ____ / ____ )

- Rework as necessary.

## *4F. Week #3: Lab Section*

### 14. Polysilicon Etch (STEPS 3.2000-3.240)

**Postbake:** 30 min @ 110°C in the oven

Because the wafers have been potentially been sitting for several days since the lithography was finished, the resist may have absorbed some water from the ambient air. To drive off any moisture, we do a 30 minute postbake @ 110°C in the standard post-bake oven.

**Plasma Poly Etch:**

This etch defines the gates and poly conductors. As was the case with poly lithography, it is very important that this etch be well controlled to produce uniform gate lengths. With care the EE410 process produces working 2 micron parts—this is where one exercises that care. The Drytek2 can use a He-Ne laser to look at the top wafer in the machine. As the poly is etched, interference minima and maxima are seen by the laser. This signal can be used for endpoint detection of the etching process. However, it is more accurate to spot the endpoint visually by watching the "bulls eye" as the wafer etches.

- Clean Drytek2 with the $O_2$ plasma descum program for 30 min.
- Season with the standard poly etch program for 30 min.
- DRYTEK 100 - poly etch conditions:
  Pressure: 150 mT
  $SF_6$ flow: 117 sccm
  F22 flow: 51 sccm
  RF power: 500 W
- Chose an electrode pair on which to etch all wafers. Electrode #3 or #4 is convenient.
- Etch T wafer to calibrate time to fully clear by visual inspection (watch the interference ring close and disappear). This should take approx. 120 to 150 seconds. Add 25% overetch and manually stop the etch.
- Time to test-wafer clear: _____ sec.
- Time with overetch: _____ sec.
- Electrode number: _____ sec.
- Set the timer to the chosen etch time and run the rest of the wafers one-at-a-time in the same electrode. Keep an eye on the flow rates, pressure, power and clearing time. Adjust the etch time if needed. The typical time to load, etch and unload is 5 minutes per wafer.
- Visual inspection: The wafers should be rust-orange where there is resist and may be light lavender where they are etched. The lavender is the field oxide and etch-produced polymers.
- Microscope inspection: Etch should look clean with minimal undercut. Active areas should be well cleared, although a tint of brownish polymer is acceptable. No poly stringers should be visible. Check this carefully on each wafer.

**Photoresist Removal:**

The resist is covered with a tough fluorinated polymer. It comes off in fresh hot piranha, but not old piranha. New piranha is a must.

- The wafers need to be cleaned using Gasonics, Recipe 013.

- Inspect each one to be sure that the resist has been removed.

### 15. PM #4: N-Select (STEPS 4.000-4.190)

**N-Select Lithography:**

N-select defines the $n_+$ source-drains and the n-poly. Remember that in this process we make both n and p poly. The litho process steps are:

- Singe & Prime in the ***yes***
- Spin coat using ***svgcoat/2*** programs 9 (no prime), 7 (1.0 μm of 3612 resist w/2 mm EBR), and 1 (prebake 90 C for 60").
- Expose on the ***asml***

  Job name: EE410R_1
  Layer ID: 5
  Layer Number: NSELECT
  Image ID: NSELECT
  Reticle ID: EE410RET3
- Post-exposure bake on ***svgdev/2*** using programs 9 (no develop) and 1 (post-expose bake@110º C for 60").
- Resist develop on ***svgdev*** using programs 3 (develop) and 1 (postbake@110º C for 60")
- Inspect. Check the alignment Verniers and record the alignment offsets. You should be able to align to within 0.5 μm from the ACTIVE level.

  Vernier #41: SELECT to ACTIVE (offset: ____ / ____ )

  Vernier #43: **SELECT to POLY** (offset: ____ / ____ )

- Rework as necessary.

**Resist hardening (below) should be performed immediately after patterning.**

## *4G. Week #4: Preparation*

### 16. N-SourceDrain Implant (STEPS 4.2000-4.260)

**Resist Hardening**

The $n_+$ implant, while of moderate energy is of high dose. This dose will burn and wrinkle unhardened resist. This UV treatment hardens the resist just enough to withstand this implant. Higher temperature postbaking over-hardens the resist, making it unnecessarily difficult to strip.

- The resist has to be hardened to avoid the resist flowing or blistering as the wafers are dosed and heated during implant.
- UV harden resist for 15 min.
- Final bake resist @ 110°C for 30 min.

### N-Source/Drain Implant:

Species: Arsenic
Energy: 180 keV
Dose: 5 □10$^{15}$ cm$^{-2}$
Beam Current: < 40 μAmp
Implant Angle: 7°

### Photoresist Removal and Clean:

The implant hardens the resist so that piranha alone cannot clear the wafers. Tests have shown that even extended times in fresh piranha are not sufficient. Therefore the resist MUST be ashed.

- Process using Standard Hard Resist Strip.

### P Blanket Implant:

The active silicon and poly not implanted with arsenic must be doped with boron. Since the arsenic went down at 5 □$^{15}$, this dose of 1 x 10$^{15}$ will not reverse the arsenic, but is enough to make good p-type contacts and okay poly.

Species: $BF_2$
Energy: 80 KeV
Dose: 1 □10$^{15}$ cm$^{-2}$
Beam Current: no limit
Implant Angle: 7°

## *4H. Week #4: Lab Section*

### 17. LTO Deposition (STEPS 4.280-4.300)

### LTO (Glass) Deposition:

This step deposits and flows PSG, while annealing the $n^+$ and $p^+$ implants. While higher temperatures could better flow the PSG, they would over-drive the boron. IMPORTANT: Do these steps without interruption. A diff-clean between PSG deposition and flow causes reentrant step profiles and severely impairs the metal step coverage.

- Process wafers through Standard Hard Resist Strip.
- Use ***tylabbpsg***
- Program "LTOPSG40" in Tylan.
- Process summary:
  - Slow push at 400°C.
  - Pump down to base pressure and perform a leak check by closing the gate valve and making sure that the system pressure doesn't rise above 100 mT.
  - Re-pump and flow 115 sccm of $O_2$.
  - Start $SiH_4$ flow of 100 sccm for enough time to deposit 50 nm of undoped $SiO_2$.
  - • Begin the doped deposition by flowing 14 sccm of $SiH_4$ and 86 sccm of $PH_3/SiH_4$. The $PH_3/SiH_4$ is a mixture of 15% $PH_3$ in $SiH_4$ which is designed to reduce the hazard of handling pure $PH_3$. A leak of $PH_3/SiH_4$ will burn which is less hazardous from a toxic standpoint than a leak of unreacted $PH_3$.
  - Purge and backfill with $N_2$ to atmospheric pressure.

- Slow pull.
- This deposition takes ~2 hr of furnace time.
- Target is ~50 nm undoped and ~550 nm doped (8% Phosphorus) oxide.

## *4I. Week #5: Preparation*

### 18. LTO Densification (STEPS 4.320-4.360)

#### Standard Pre-Diffusion Clean

#### LTO (Glass) Densification

- Program "WET950" in Tylan. Reflow Time = 30 min.
- Use ***tylan1*** ot ***tylan2***
- Process summary:
  - Slow push at 800°C.
  - Ramp to 950°C in $N_2$ (30 min).
  - Reflow: Steam (30 min). Heavily doped LTO (such as the 8% PSG that we are using) will become somewhat "plastic" at 950°C in steam. This will tend to smooth out any rough edges over poly steps and will ultimately improve the shape of the steps that the aluminum metallization has to cover. The steam is bracketed by dry oxidations.
  - Ramp down in $N_2$ (20 min).
  - Slow pull.
- This reflow takes ~1 hr and 30 min of furnace time.

### 19. PM #5: Contact Holes (STEPS 5.000-5.190)

#### Contact Lithography:

Contact lithography is often difficult since it is a dark field alignment and is over the LTO which is rough and shows a "starry sky" in dark field.

- Singe & Prime in the ***yes***
- Spin coat using ***svgcoat/2*** programs 9 (no prime), 7 (1.0 μm of 3612 resist w/2 mm EBR), and 1 (prebake 90 C for 60").
- Expose on the ***asml***

  Job name: EE410R_1
  Layer ID: 6
  Layer Number: CONTACT
  Image ID: CONTACT
  Reticle ID: EE410RET3
- Post-exposure bake on ***svgdev/2*** using programs 9 (no develop) and 1 (post-expose bake@110º C for 60").
- Resist develop on ***svgdev*** using programs 3 (develop) and 1 (postbake@110º C for 60")
- Inspect. Check the alignment Verniers and record the alignment offsets. You should be able to align to within 0.5 μm from the ACTIVE level.

Vernier #51: CONT to ACTIVE (offset: ____ / ____ )

Vernier #53: **CONT to POLY** (offset: ____ / ____ )

- Rework as necessary.

## *4J. Week #5: Lab Section*

### 20. Oxide Etch (STEPS 5.200-5.260)

**Postbake:** 30 min @ 110°C in the oven

**Plasma Contact Etch:**

For the contacts we do not etch wet. While we would like sloped contact walls for good aluminum coverage, the contact holes are small and close together, so we need steep sidewalls. Also, PSG can etch laterally very fast, so we choose a plasma etch.

- Note: **Always run the AMT for 10 to 15 min prior to processing any device wafers.** This conditions the chamber and produces a more uniform etch.
- Also, always **review the program** to be sure the setup has not been changed. **Record the actual readouts** on the runsheet (see below).
- Note: This process etches **undoped and undensified LTO** ~40 nm/min, silicon > 5 nm/min.
- Etch T test wafer first. The Nano-spec reading should be "less than 20 A". Etch the rest of the wafers for the same time.
- AMT - Oxide etch conditions:

  Trans Power: 1100 W (typical) _____(actual)
  Rfld Power: 20 W (typical) _____(actual)
  Bias: - 535 V _____(actual)
  $O_2$ flow: 6 sccm (Gas 1) _____(actual)
  CHF3 flow: 86 sccm (Gas 2) _____(actual)
  Pressure: 40 mT _____(actual)
  Hexode Temp: 22°C _____(actual)
  Time: (To be calculated) _____(actual)
- Check etched areas with the Nanospec to insure that etching is complete.

**Photoresist Removal and Clean:**

The oxide etch hardens the resist so that piranha alone cannot clear the wafers. Therefore the resist must be ashed.

- Process using Standard Hard Resist Strip.
- Inspect to be sure that the resist has been removed.

## *4K. Week #6: Preparation*

### 21. Metal Deposition (STEPS 5.300-5.320)

**Aluminum/Silicon Alloy Deposition:**

It is important when depositing contacts to have clean silicon at the bottom of the cuts. To minimize oxide we do a brief HF dip, and a sputter clean when the wafers are in vacuum.

- Process using Standard Pre-Metal Deposition Clean
- Metal Deposition should be preceded by in-situ sputter clean
- Deposit 1.0 μm Al/1%Si in Gryphon sputtering system. Program 1 Standard Al/Si Deposition

### 22. PM #6: Metal (STEPS 6.120-6.170)

**Aluminum Lithography:**

The aluminum lithography is generally the most difficult since it over both the rough the LTO and the rough aluminum. For aluminum lithography the exposure will be substantially less than it has been for the previous layers because of the high reflectivity of the aluminum. To protect our wafers, we will use a thicker 1.6 um resist since the Al etch is not very selective to it. Note the different programs for the resist coat and develop.

- Singe & Prime in the ***yes***
- Spin coat using ***svgcoat/2*** programs 9 (no prime), 7 (1.0 μm of 3612 resist w/2 mm EBR), and 1 (prebake 90 C for 60").
- Expose on the ***asml***

  Job name: EE410R_1
  Layer ID: 4
  Layer Number: METAL
  Image ID: METAL
  Reticle ID: EE410RET2
- Post-exposure bake on ***svgdev/2*** using programs 9 (no develop) and 1 (post-expose bake@110º C for 60").
- Resist develop on ***svgdev*** using programs 3 (develop) and 1 (postbake@110º C for 60")
- Inspect. Check the alignment Verniers and record the alignment offsets. You should be able to align to within 0.5 μm from the ACTIVE level.

  Vernier #61: METAL1 to ACTIVE (offset: ____ / ____ )

  Vernier #63: METAL1 to POLY (offset: ____ / ____ )

  Vernier #65: **METAL1 to CONT** (offset: ____ / ____ )

- Rework as needed.

## 4L. Week #6: Lab Section

### 23. Metal Etch (STEPS 6.200-6.240)

**Postbake:** 30 min @ 110°C in the oven

**Dry Aluminum Etch:**
Aluminum can be etched wet or dry. In this process we use an anisotropic dry etch. The wafers are etched in the Precision 5000. The recipe that will be used is CHA.METAL and to etch about 1um will take 80 sec. This recipe uses chlorine gas to etch the Al. More details will be provided later.

**Photoresist Removal:**
Use Standard Metal Layer Resist Strip.

## 4M. Final Preparation

### 24. Anneal/Alloy (STEPS 6.260-6.300)

**Metal Clean:**
We cannot do the diff-clean sequence since it would also remove the aluminum, so we have a solvent-based version of that.

- Repeat the previous two steps using the PRX-1000 Clean Bath, i.e., dump rinse, spin dry, dump rinse, and spin dry after the clean bath.
- Load wafers into ***tylanfga*** immediately after clean step.

**Anneal and Alloy:**
The aluminum is in contact with the silicon, but a better electrical contact is made if we react the junction slightly. This step also hydrogen terminates some of the $Q_f$ in the gate oxide.

- Use ***tylanfga***
- Program "FGA400" in Tylan.
- Forming gas is a mixture of 10% $H_2$ in $N_2$. This step reduces the interface trap density by allowing the hydrogen to react with any dangling silicon bonds at the $Si/SiO_2$ interface, reduces radiation damage to the oxide induced during the sputtering process, and causes the aluminum to make good electrical contact to the underlying silicon.
- Process summary:
    - Slow push at 400°C.
    - Anneal in forming gas (45 min).
    - Slow pull.
- This process takes ~1 hr.

## *RUN IS COMPLETE!!!!!!*

## ***SECTION 5***

## EE410 CMOS PROCESS SCHEDULE

### Week 1: Preparation

1. Wafer Start: Starting material is n-type silicon [STEP 00.000]
    - Standard piranha clean

2. Photomask #0: Zero level marks [STEPS 0.100-0.190]
    - Singe and prime (***yes*** oven)
    - Resist coat (***svgcoat/2,*** programs 9,7,1)
    - Expose (***asml,*** with reticle 45023981A009, Job Name: EE410R_1)
    - Post exposure bake (***svgcoat/2,*** programs 9,1)
    - Develop (***svgdev/2,*** program 3,1)
    - Inspect/rework as needed
    - Postbake @110C, 30 min.

3. Silicon etch [STEPS 0.200-0.240]
    - Hand scribe wafer ID
    - Silicon Oxide etch (***amtetcher***, program 4 for 5 minutes)
    - Standard Hard Resist Strip (***gasonics***, program 013, ***wbnonmetal***, 10 min piranha)

4. Blanket Implant [STEPS 0.300-0.360]
    - Standard pre-diffusion clean (***wbdiff)***
    - Implant: 100 keV, P31, 1.75 X $10^{12}$ cm $^{-2}$

5. Field Oxidation [STEPS 0.360-0.380]
    - Standard pre-diffusion clean (***wbdiff)***
    - Field Oxidation (***tylan1/2***: Ramped process 10' dry/100' steam/10' dry @ 1000°C, ≈ 5000Å
    - Inspection/thickness measurement

### Week 1: Lab Section

6. Photomask #1: Active Area [STEPS 1.000-1.190]
    - Singe and prime (***yes*** oven)
    - Resist coat (***svgcoat/2,*** programs 9,7,1)
    - Expose (***asml,*** with reticle EE410RET1, Job Name: EE410R_1)
    - Post exposure bake (***svgcoat/2,*** programs 9,1)
    - Develop (***svgdev/2,*** program 3,1)
    - Inspect/rework as needed

- Postbake @110C, 30 min.

7. Active Area Etch (FOX definition) [STEPS 1.200-1.240]
   - Descum (***drytek2***, 30 sec)
   - $SiO_2$ etch in 6:1 buffered HF (***wbnonmetal)***

**Week 2: Preparation**

8. Sacrificial Ox [STEPS 1.250-1.340]
   - Standard Hard Resist Strip (***gasonics***, program 013, ***wbnonmetal***, 10 min piranha)
   - Standard pre-diffusion clean (***wbdiff)***
   - Sacrificial Oxidation (***tylan1/2***: Ramped process 5' dry/12' steam/5' dry 900°C, ≈ 400Å
   - Inspection/Thickness measurement

9. Photomask #2: P-Well [STEPS 2.000-2.190]
   - Singe and prime (***yes*** oven)
   - Resist coat (***svgcoat/2,*** programs 9,7,1)
   - Expose (***asml,*** with reticle EE410RET1, Job Name: EE410R_1)
   - Post exposure bake (***svgcoat/2,*** programs 9,1)
   - Develop (***svgdev/2,*** program 3,1)
   - Inspect/rework as needed
   - Postbake @110C, 30 min.

10. P-Well Double Implant: [STEP 2.200]
    - 180 keV, B11, $5.0 \cdot 1012$ $cm^{-2}$ and 50 keV, B11, $1.4 \cdot 10^{12}$ $cm^{-2}$

**Week 2: Lab Section**

11. P-well drive-in [STEPS 2.210-2.260]
    - Standard Hard Resist Strip (***gasonics***, program 013, ***wbnonmetal***, 10 min piranha)
    - Standard pre-diffusion clean (***wbdiff)***
    - P-Well Drive-In: (***tylan1/2***) 60' $N_2$ @ 1000°C

**Week 3: Preparation**

12. Gate Oxidation/Poly Deposition [STEPS 2.300-2.420]
    - Standard pre-diffusion clean (***wbdiff)***
    - Sacrificial oxide strip (***wbdiff)***
    - Gate Oxidation: 400Å
    - Polysilicon Deposition: LPCVD @ 560°C, ≈ 5000Å
    - Inspection/polysilicon thickness measurements

13. Photomask #3: Polysilicon [STEPS 3.000-3.190]
    - Singe and prime (***yes*** oven)
    - Resist coat (***svgcoat/2,*** programs 9,7,1)
    - Expose (***asml,*** with reticle EE410RET2, Job Name: EE410R_1)
    - Post exposure bake (***svgcoat/2,*** programs 9,1)
    - Develop (***svgdev/2,*** program 3,1)
    - Inspect/rework as needed
    - Postbake @110C, 30 min.

**Week 3: Lab Section**

14. Poly Etch [STEPS 3.200-3.240]
    - Postbake @ 110°C, 30'
    - Descum (***drytek2***: $O_2$ descum, CF4/O2 etch)
    - Plasma poly etch (***drytek2***: SF6/F22)
    - Standard Hard Resist Strip (***gasonics***, program 013, ***wbnonmetal***, 10 min piranha)

15. Photomask #4 – N-SELECT [STEPS 4.000-4.190]
    - Singe and prime (***yes*** oven)
    - Resist coat (***svgcoat/2,*** programs 9,7,1)
    - Expose (***asml,*** with reticle EE410RET2, Job Name: EE410R_1)
    - Post exposure bake (***svgcoat/2,*** programs 9,1)
    - Develop (***svgdev/2,*** program 3,1)
    - Inspect/rework as needed
    - Postbake @110C, 30 min.

**Week 4: Preparation**

16. N- Source/Drain Implant [STEPS 4.200-4.260]
    - Resist hardening: UV bake 15 min, final bake 30 min @ 110°C (should be performed immediately after developing)
    - N-Source/Drain Implant: 180 keV, As75, 5 x $10^{15}$ $cm^{-2}$
    - Standard Hard Resist Strip (***gasonics***, program 013, ***wbnonmetal***, 10 min piranha)
    - P Blanket Implant: 80 keV, $BF_2^{49}$, 1 x $10^{15}$ $cm^{-2}$

**Week 4: Lab Section**

17. LTO Deposition [STEPS 4.280-4.300]
    - Standard pre-diffusion clean (***wbdiff)***
    - LTO Deposition (***tylanbpsg***, program "LTOPSG40"): LPCVD @ 400°C, ≈ 6000Å

- Oxide thickness measurements

**Week 5: Preparation**

18. LTO Densification [STEPS 4.320-4.260]
    - Standard pre-diffusion clean (***wbdiff)***
    - LTO Densification (***tylan1/2***, program 950AN): Ramped process 30' $N_2$ @ 950°C

19. Photolithography #5 – Contact Holes [STEPS 5.000-5.190]
    - Singe and prime (***yes*** oven)
    - Resist coat (***svgcoat/2,*** programs 9,7,1)
    - Expose (***asml,*** with reticle EE410RET3, Job Name: EE410R_1)
    - Post exposure bake (***svgcoat/2,*** programs 9,1)
    - Develop (***svgdev/2,*** program 3,1)
    - Inspect/rework as needed
    - Postbake @110C, 30 min.

**Week 5: Lab Section**

20. Plasma Oxide Etch [STEPS 5.200-5.260]
    - Postbake @ 110°C, 30'
    - $SiO_2$ RIE in AMT 8100: $CHF_3/O_2$
    - Standard Hard Resist Strip (***gasonics***, program 013, ***wbnonmetal***, 10 min piranha)

**Week 6: Preparation**

21. Metal Deposition [STEPS 5.300-5.320]
    - Standard pre-diffusion clean (***wbdiff)***
    - Al/Si Deposition in Gryphon Sputtering System: ≈ 10000Å
    -
22. Photolithography #6 – Metal [STEPS 6.000-6.190]
    - Singe and prime (***yes*** oven)
    - Resist coat (***svgcoat/2,*** programs 9,8,2)
    - Expose (***asml,*** with reticle EE410RET2, Job Name: EE410R_1)
    - Post exposure bake (***svgcoat/2,*** programs 9,2)
    - Develop (***svgdev/2,*** program 4,2)
    - Inspect/rework as needed
    - Postbake @110C, 30 min.

**Week 6: Lab Section**

23. Metal Etch [STEPS 6.210-6.240]
    - Postbake @ 110°C, 30'

- Al/Si Dry Etch in P-5000: $Cl_2$
- Etch Passivation (***wbmetal***, dump rinse for 6 cycles, spin-rinse-dry)
- Std Metal Resist Strip (***gasonics***, program 013; ***wbmetal***, PRX-127 for 10 min)

## Final Preparation

24. Anneal/Alloy [STEPS 6.260-6.300]
    - Pre-furnace Metal Clean (***wbmetal***, PRX-1000 @ 40°C, 10', spin-rinse-dry)
    - Anneal/Alloy (***tylanfga)***: 45' forming gas (10% $H_2$ in $N_2$) @ 400°C

## WEEK #1: PREPARATION

## *1. Wafer Start*

**WAFER START** - Starting material is n-type silicon (SNF Stockroom code: C Prime.)

**STEP 00.00 – STANDARD PIRANHA CLEAN**
***wbnonmetal*** – piranha clean for 20 min, rinse, spin-rinse-dry

Date _____Time _____Operator _____

Comments_____

## *2. PM #0: Zero Level Marks*

**PHOTOMASK #0- ZERO LEVEL MARKS**
All device wafers plus T1-T4. Use T1 and T2 to optimize focus and exposure.

**STEP 0.100 - SINGE & PRIME**
***yes*** standard oven singe/HMDS prime

Date _____Time _____Operator _____

Comments_____

**STEP 0.120 - RESIST SPIN COAT**
***svgcoat*** programs 9 (no prime), 7 (coat 1.0 μm of 3612 resist), and 1 (prebake).

System used: ❑***svgcoat*** ❑***svgcoat2***

Date_____ Time _____ Operator_____

Comments_____

**STEP 0.140 – NON-ALIGNED EXPOSURE**
Expose using asml stepper:
Job name: EE410R_1
Layer ID: 0
Layer Number: 0
Image ID: PM
Reticle ID 45023981A009

Exposure used:_____

Date _____Time _____Operator _____

Comments_____

**STEP 0.160 – POST EXPOSURE BAKE**
***svgdev*** programs 9 (no develop) and 1 (bake)

System: ❑***svgdev*** ❑***svgdev2***

Date _____ Time _____Operator _____

Comments_____

**STEP 0.170 - RESIST DEVELOP**
***svgdev*** programs 3 (develop) and 1 (postbake)

System: ❑***svgdev*** ❑***svgdev2***

Date _____ Time _____Operator _____

Comments_____

**STEP 0.180 - INSPECTION**
Visual microscope inspection. Check for defects and alignment/exposure quality.

Wafers inspected ____ ____ ____ ____ ____

Date _____ Time _____Operator _____

Comments_____

REWORK DONE? ❑***yes*** ❑***no***

Wafer #'s reworked: _____
If yes, attach REWORK sheet here.

**STEP 0.190 - POSTBAKE**
***110° C oven*** for 30 min,

Date _____ Time _____Operator _____

Comments_____

## *3. Zero Level Silicon Etch*

**STEP 0.200 – SCRIBE**
Hand-scribe wafers near the flat. Angle the lettering so that no lines are drawn perpendicular or parallel to the flat. Scribe only deep enough to remove resist. Scribed lettering will be etched in the next step.

**STEP 0.220 – SILICON ETCH**
***amtetcher***, Program 4 for 0:05:00.

Date_____ Time _____Operator _____

Comments_____

**STEP 0.230 – STD HARD RESIST STRIP: RESIST ASH**
***gasonics***, program 013

Date_____ Time _____Operator _____

Comments_____

**STEP 0.240 – STD HARD RESIST STRIP: PIRANHA**
***wbnonmetal***, Piranha @ 120°C, 10', rinse, spin dry

Date_____ Time _____Operator _____

Comments_____

**WEEK #1: LAB SECTION**

## *4. Blanket Implant*

**STEP 0.300 - STANDARD PRE-DIFFUSION CLEAN**
***wbdiff***, 4:1 H2SO4:H2O2 @ 90°C, 10', rinse;
50:1 DI:HF @ Room Temp, 30 sec, rinse;
5:1:1 DI:H2O2:HCl @ 70°C, 10', rinse, spin dry

Date _____ Time _____ Operator_____

Comments_____

**STEP 0.320 - BLANKET SUBSTRATE IMPLANT**
***Implant Services:*** , 100 keV, P31, 1.75x$10^{12}$ $cm^{-2}$.

Date Sent _____ Date Returned _____

Vendor: _____

Comments_____

**STEP 0.340 - STANDARD PRE-DIFFUSION CLEAN**
***wbdiff***, 4:1 H2SO4:H2O2 @ 90°C, 10', rinse;
50:1 DI:HF @ Room Temp, 30 sec, rinse;
5:1:1 DI:H2O2:HCl @ 70°C, 10', rinse, spin dry

Date _____ Time _____ Operator _____

Comments_____

## *5. Field Oxidation*

**STEP 0.360 - FIELD OXIDATION**
Ramped process 10'D/100'W/10'D @ 1000°C, ≈ 5000Å,

***tylan1 or 2:*** Program 'FIELDOX' on EE410 Disc.

Date _____ Time _____ Operator _____

System used _____

**STEP0.380 – INSPECTION: THICKNESS MEASUREMENT**
Use Nanospec, program 1 (oxide) to measure T1 oxide thickness and uniformity.

System used: ❑***nanospec*** ❑***nanospec2***
Wfr#____ T_____ C_____ B_____ R_____ L_____

Wfr#____ T_____ C_____ B_____ R_____ L_____

Wfr#____ T_____ C_____ B_____ R_____ L_____

Wfr#____ T_____ C_____ B_____ R_____ L_____

Thk %Uniformity _____

Comments_____

## *6. PM #1: Active Area*

Select two wafers (T1,T2) to be used as test wafers. These will undergo all processing, but will be used to optimize the Focus and Exposure Matrix (FEM) at all photolithography steps and for etch rates. More blank wafers will be included later for additional film thickness and etch rate measurements. Indicate ID's of wafers to be used as test wafers T1 and T2.

T1 _____ T2 _____

**PHOTOMASK #1- ACTIVE AREA**
Use T1 and T2 to optimize focus and exposure.

**STEP 1.000 - SINGE & PRIME**
***yes*** standard oven singe/HMDS prime

Date _____Time _____Operator _____

Comments_____

**STEP 1.120 - RESIST SPIN COAT**
***svgcoat*** programs 9 (no prime), 7 (coat 1.0 μm of 3612 resist), and 1 (prebake).

System used: ❑***svgcoat*** ❑***svgcoat2***

Date_____ Time _____ Operator_____

Comments_____

**STEP 1.140 - ALIGNED EXPOSURE**
Expose using asml stepper:
Job name: EE410R_1
Layer ID: 1
Layer Number: ACTIVE
Image ID: ACTIVE
Reticle ID: EE410RET1

Exposure used:_____

Date _____Time _____Operator _____

Comments_____

**STEP 1.160 – POST EXPOSURE BAKE**
***svgdev*** programs 9 (no develop) and 1 (bake)

System: ❑***svgdev*** ❑***svgdev2***

Date _____ Time _____Operator _____

Comments_____

**STEP 1.170 - RESIST DEVELOP**
Develop using SVG Dev track, programs 3 (develop) and 1 (bake)

System: ❑***svgdev*** ❑***svgdev2***

Date _____ Time _____Operator _____

Comments_____

**STEP 1.180 - INSPECTION**
Visual microscope inspection. Check for defects and alignment/exposure quality.

Wafers inspected ____ ____ ____ ____ ____

Date _____ Time _____Operator _____

Comments_____

**STEP 1.190 - POSTBAKE**
Bake in the 110 C postbake oven for 30 minutes.

Date _____ Time _____Operator _____

Comments_____

REWORK DONE? ❑***yes*** ❑***no***

Wafers reworked: _____
If yes, attach REWORK sheet here.

## ***7. Active Area Etch***

**STEP 1.200 - DESCUM**
***drytek2***, Program 'DESCUM' (100sccm O2, 150mT, 500W, 30 sec)

Date _____ Time _____Operator _____

Comments_____

**STEP 1.220 - SiO2 ETCH**
All device wafers plus T1 and T2. Use TI to establish etch time

***wbdiff***, in 6:1 buffered HF, 400-600 sec, rinse, spin dry

Etch Times used: _____

Date_____ Time _____Operator _____

**STEP 1.240 - INSPECTION: THICKNESS MEASUREMENT**
Use Nanospec program 7 (thin oxide) to measure T1 to ensure complete oxide removal (flat down.)

System used: ❑***nanospec*** ❑***nanospec2***

T_____C_____B_____R_____L_____

Comments_____

**WEEK #2: PREPARATION**

## ***8. Sacrificial Oxidation***

**Step 1.250 – STD HARD RESIST STRIP: RESIST ASH**
***gasonics***, program 013

Date_____ Time _____Operator _____
Comments_____

**STEP 1.260 - STD HARD RESIST STRIP: PIRANHA**
***wbnonmetal***, Piranha @ 120°C, 10', rinse, spin dry

Date_____ Time _____Operator _____

Comments_____

**STEP 1.300 - STANDARD PRE-DIFFUSION CLEAN**
***wbdiff***, 4:1 H2SO4:H2O2 @ 90°C, 10', rinse;
50:1 DI:HF @ Room Temp, 30 sec, rinse;
5:1:1 DI:H2O2:HCl @ 70°C, 10', rinse, spin dry

Date_____ Time _____Operator _____

Comments_____

**STEP 1.320 - SACRIFICIAL OXIDATION**
Ramped process 5'D/12'W/5'D @ 900°C, ≈ 400Å

***tylan1 or 2***, Program 'GATEOX' on EE410 disk

Date _____ Time _____Operator _____

Comments_____

**STEP 1.340 – INSPECTION: THICKNESS MEASUREMENT**
Use Nanospec Thick Ox program to inspect T1 for oxide thickness and uniformity. Use F-1 region on selected die.

System used: ❑***nanospec*** ❑***nanospec2***

T_____C_____B_____R_____L_____

% Unifomity _____

Comments_____

Use Nanospec program 7 (Thin Ox) to inspect T1 for oxide thickness and uniformity. Use F-2 region on selected die.

System used: ❑***nanospec*** ❑***nanospec2***

T_____C_____B_____R_____L_____

% Unifomity _____

Comments_____

Comments _____

## *9. PM #2: P-Well*

**PHOTOMASK #2 – P-WELL**
Use T1 and T2 to optimize focus and exposure matrix (FEM).

**STEP 2.000 - SINGE & PRIME**
***yes*** standard oven singe/HMDS prime

Date _____ Time _____Operator _____

Comments_____

**STEP 2.120 - RESIST SPIN COAT**
***svgcoat*** programs 9 (no prime), 7 (coat 1.0 μm of 3612 resist), and 1 (prebake).

System used: ❑***svgcoat*** ❑***svgcoat2***

Date _____ Time _____Operator _____

Comments _____

**STEP 2.140 - ALIGNED EXPOSE**
Expose using asml stepper:
Job name: EE410R_1
Layer ID: 2
Layer Number: PWELL
Image ID: PWELL
Reticle ID: EE410RET1

Date _____ Time _____ Operator _____

Exposure used:_____

Comments_____

**STEP 2.160 – POST EXPOSURE BAKE**
***svgdev*** programs 9 (no develop) and 1 (bake)

System: ❑***svgdev*** ❑***svgdev2***

Date _____ Time _____Operator _____

Comments_____

**STEP 2.170 - RESIST DEVELOP**
Develop using SVG Dev track, programs 3 (develop) and 1 (bake)

System used: ❑***svgdev*** ❑***svgdev2***

Date_____Time _____Operator _____

Comments_____

**STEP 2.180 - INSPECTION**
Visual microscope inspection. Check for defects and alignment/exposure quality.

Wafers inspected ____ ____ ____ ____ ____

**STEP 2.190 - POSTBAKE**
Bake in the 110 C postbake oven for 30 minutes.

Date _____ Time _____Operator _____

Comments_____

**REWORK DONE?** ❑***yes*** ❑***no***

Wafers reworked: _____

If yes, attach REWORK sheet here.

## *10. Double-Well Implant*

**STEP 2.200 - P-WELL DOUBLE IMPLANT**
***Implant Services:*** 180 KeV, B11, $5.0 \times 10^{12}$ $cm^{-2}$; and 50 KeV, B11, $1.4 \times 10^{12}$ $cm^{-2}$

Date Sent _____ Date Returned _____

Vendor: _____

Comments _____

## WEEK #2: LAB SECTION

## *11. P-Well Drive-in*

**Step 2.210 – STD HARD RESIST STRIP: RESIST ASH**
***gasonics***, program 013

Date_____ Time _____Operator _____

Comments_____

**STEP 2.220 - STD HARD RESIST STRIP: PIRANHA**
***wbnonmetal***, Piranha @ 120°C, 10', rinse, spin dry

Date_____ Time _____Operator _____

Comments_____

**STEP 2.240 - STANDARD PRE-DIFFUSION CLEAN**
***wbdiff***, 4:1 H2SO4:H2O2 @ 90°C, 10', rinse;
50:1 DI:HF @ Room Temp, 30 sec, rinse;
5:1:1 DI:H2O2:HCl @ 70°C, 10', rinse, spin dry

Date_____ Time _____Operator _____

Comments_____

**STEP 2.260 - P-WELL DRIVE IN**
60' Ar @ 1000°C

**CHECK WITH SNF PROCESS STAFF BEFORE RUNNING**

***Tylan1 or 2***, Program 'PWELLDI' on EE410 disk

Date_____ Time _____Operator _____

Comments_____

## WEEK #3: PREPARATION

## *12. Gate Oxidation/Poly Deposition*

**STEP 2.300 – STANDARD PRE-DIFFUSION CLEAN**
Add in a clean blank test wafer, T3, for Gate Ox measurement.

***wbdiff***, 4:1 H2SO4:H2O2 @ 90°C, 10', rinse;
50:1 DI:HF @ Room Temp, 30 sec, rinse;
5:1:1 DI:H2O2:HCl @ 70°C, 10', rinse, spin dry

Date_____ Time _____Operator _____

Comments_____

**STEP 2.320 - SACRIFICIAL OXIDE STRIP**
This is a long slow, but clean etch.

***wbdiff*** 50:1 DI:HF @ Room Temp, ~12 mins; rinse, spin dry

Date_____ Time _____Operator _____

Comments_____

**STEP 2.340 - GATE OXIDATION**
Include T3 (blank). Ramped process 5'D/12'W/5'D @ 900°C, ≈ 400Å

NOTE: Run TLCCLEAN program on tylan1/2 to clean tube before GATEOX. This will take about 4 hours to complete. Wafers must go immediately into tylanpoly after GateOx with no cleaning steps. This is to ensure contamination is minimal.

***tylan1 or 2***, Program 'GATEOX' on EE410 disk

Date _____ Time _____Operator _____

Comments_____

**STEP 2.360 – INSPECTION: THICKNESS MEASUREMENT**
Use Nanospec program 7 (Thin Ox) to inspect T3 for oxide thickness and uniformity.

System used: ❑***nanospec*** ❑***nanospec2***

T_____C_____B_____R_____L_____

% Unifomity _____

Comments_____

**STEP 2.400 - POLYSILICON DEPOSITION**

Removed Gate Ox Test wafer. LPCVD @ 560°C, ≈ 5000Å

***tylanpoly*** Program AMOR4006 on EE410 disk.

Date _____ Time _____Operator _____

Comments_____

**STEP 2.420 – INSPECTION: THICKNESS MEASUREMENT**
Use Nanospec program 4 (Polysilicon on Oxide) to inspect T3 for poly thickness and uniformity. After this, T3 is no longer needed.

System used: ❑***nanospec*** ❑***nanospec2***

T_____C_____B_____R_____L_____

% Unifomity _____

Comments_____

## *13. PM #3: Polysilicon*

**PHOTOMASK #3 - POLYSILICON**
Use T1 and T2 to optimize focus and exposure.

**STEP 3.000 - SINGE & PRIME**
***yes*** standard oven singe/HMDS prime

Date _____ Time _____Operator _____

Comments_____

**STEP 3.120 - RESIST SPIN COAT**
***svgcoat*** programs 9 (no prime), 7 (coat 1.0 μm of 3612 resist), and 1 (prebake).

System used: ❑***svgcoat*** ❑***svgcoat2***

Date _____ Time _____Operator _____

Comments _____

**STEP 3.140 - ALIGNED EXPOSE**
Expose using asml stepper:
Job name: EE410R_1
Layer ID: 3
Layer Number: POLY
Image ID: POLY
Reticle ID: EE410RET2

Date _____ Time _____ Operator _____

Comments_____

**STEP 3.160 – POST EXPOSURE BAKE**
***svgdev*** programs 9 (no develop) and 1 (bake)

System: ❑***svgdev*** ❑***svgdev2***

Date _____ Time _____Operator _____

Comments_____

**STEP 3.170 - RESIST DEVELOP**
Develop using SVG Dev track, programs 3 (develop) and 1 (bake)

System used: ❑***svgdev*** ❑***svgdev2***

Date_____Time _____Operator _____

Comments_____

**STEP 3.180 - INSPECTION**
Visual microscope inspection. Check for defects and alignment/exposure quality.

Wafers inspected ____ ____ ____ ____ ____

Date _____ Time _____Operator _____

Comments _____

**STEP 3.190 - POSTBAKE**
Bake in the 110 C postbake oven for 30 minutes.

Date _____ Time _____Operator _____

Comments_____

**REWORK DONE?** ❑***yes*** ❑***no***

Wafers reworked: _____

If yes, attach REWORK sheet here.

## WEEK #3: LAB SECTION

## *14. Polysilicon Etch*

**STEP 3.200 - POSTBAKE**
Bake in the 110 C postbake oven for 30 minutes.

Date _____ Time _____Operator _____

Comments_____

**STEP 3.210 - DESCUM**
***drytek2***, Program 'DESCUM' (100sccm O2, 150mT, 500W, 30 sec)

Date _____ Time _____Operator _____

Comments_____

**STEP 3.220 - POLY ETCH**
Use T1 to establish etch rate, ~3:30mins

***drytek2***, Program 'POLY ETCH' (117sccm SF6, 51sccm F22, 150mT, 400W)

Date _____ Time _____Operator _____

Comments_____

**Step 3.230 – STD HARD RESIST STRIP: RESIST ASH**
***gasonics***, program 013

Date_____ Time _____Operator _____

Comments_____

**STEP 3.240 - STD HARD RESIST STRIP: PIRANHA**
***wbnonmetal***, Piranha @ 120°C, 10', rinse, spin dry

Date_____ Time _____Operator _____

Comments_____

## *15. PM #4: N-Select*

**PHOTOMASK #4 – N-SELECT**
Use T1 and T2 to optimize focus and exposure.

**STEP 4.000 - SINGE & PRIME**
***yes*** standard oven singe/HMDS prime

Date _____ Time _____Operator _____

Comments_____

**STEP 4.120 - RESIST SPIN COAT**
***svgcoat*** programs 9 (no prime), 7 (coat 1.0 μm of 3612 resist), and 1 (prebake).

System used: ❑***svgcoat*** ❑***svgcoat2***

Date _____ Time _____Operator _____

Comments _____

**STEP 4.140 - ALIGNED EXPOSE**
Expose using asml stepper:
Job name: EE410R_1
Layer ID: 5
Layer Number: NSELECT
Image ID: NSELECT

Date _____ Time _____ Operator _____

Exposure used:_____

Comments_____

**STEP 4.160 – POST EXPOSURE BAKE**
***svgdev*** programs 9 (no develop) and 1 (bake)

System: ❑***svgdev*** ❑***svgdev2***

Date _____ Time _____Operator _____

Comments_____

**STEP 4.170 - RESIST DEVELOP**
Develop using SVG Dev track, programs 3 (develop) and 1 (bake)

System used: ❑***svgdev*** ❑***svgdev2***

Date_____Time _____Operator _____

Comments_____

**STEP 4.180 - INSPECTION**
Visual microscope inspection. Check for defects and alignment/exposure quality.

Wafers inspected ____ ____ ____ ____ ____

Date _____ Time _____Operator _____

Comments _____

**STEP 4.190 - POSTBAKE**
Bake in the 110 C postbake oven for 30 minutes.

Date _____ Time _____Operator _____

Comments_____

**REWORK DONE?** ❑***yes*** ❑***no***

Wafers reworked: _____

If yes, attach REWORK sheet here.

## WEEK #4: PREPARATION

## *16. N-Source/Drain Implant*

**STEP 4.200 - RESIST HARDENING (for implantation)**
UV exposure 15 mins, final bake 30 mins @ 110C. (Perform immediately after develop).

Date _____ Time _____Operator _____

Comments_____

**STEP 4.210 - N-SOURCE/DRAIN**
***Implant Service:*** 180 KeV, As75, 5.0x$10^{15}$ $cm^{-2}$

Date Sent _____ Date Returned _____

Vendor: _____

Comments _____

**Step 4.22 – STD HARD RESIST STRIP: RESIST ASH**
***gasonics***, program 013

Date_____ Time _____Operator _____

Comments_____

**STEP 4.240 - STD HARD RESIST STRIP: PIRANHA**
***wbnonmetal***, Piranha @ 120°C, 10', rinse, spin dry

Date_____ Time _____Operator _____

Comments_____

**STEP 4.260 - P-BLANKET IMPLANT**
***Implant Service:*** 80 KeV, BF249, 1x$10^{15}$ $cm^{-2}$

Date Sent _____ Date Returned _____

Vendor: _____

Comments _____

## WEEK #4: LAB SECTION

## *17. LTO Deposition*

**STEP 4.280 - STANDARD PRE-DIFFUSION CLEAN**
Add in a blank test wafer, T4, for LTO thickness/densification measurement.

***wbdiff***, 4:1 H2SO4:H2O2 @ 90°C, 10', rinse;
50:1 DI:HF @ Room Temp, 30 sec, rinse;
5:1:1 DI:H2O2:HCl @ 70°C, 10', rinse, spin dry

Date_____ Time _____Operator _____

Comments_____

**STEP 4.300 - LTO DEPOSITION**
Include T4. Undoped/Doped, LPCVD @ 400°C, ≈ 6000Å

***tylanbpsg***, Program 'LTOPSG40' on EE410 disk

Date_____ Time _____Operator _____

Comments_____

## WEEK #5: PREPARATION

## *18. LTO Densification*

**STEP 4.320 - STANDARD PRE-DIFFUSION CLEAN**
Note: Pre-Diffusion clean may be omitted if wafers go directly from LTO dep to LTO densify. Less than one hour must be between the two steps. Include T4 for LTO measurement after Densification.

***wbdiff***, 4:1 H2SO4:H2O2 @ 90°C, 10', rinse;
50:1 DI:HF @ Room Temp, 30 sec, rinse;

5:1:1 DI:H2O2:HCl @ 70°C, 10', rinse, spin dry

Date_____ Time _____Operator _____

Comments_____

**STEP 4.340 LTO DENSIFICATION**
Include T4. Ramped process 30' $N_2$ @ 950°C

***tylan1 or 2***, Program '950AN' on ANNEAL disk

Date _____ Time _____Operator _____

Comments_____

**STEP 4.360 – INSPECTION: THICKNESS MEASUREMENT**
Use Nanospec program 1 (Oxide on silicon) to inspect T4 wafer for oxide thickness and uniformity. KeepT4 for etch rates.

System used: ❑***nanospec*** ❑***nanospec2***

T_____C_____B_____R_____L_____

% Unifomity _____

Comments_____

## *19. PM #5: Contact Holes*

**PHOTOMASK #5 – CONTACT HOLES**
Use T1 and T2 to optimize focus and exposure. T4 may be used as a test wafer at $SiO_2$ RIE and so needs to be blind patterned.

**STEP 5.000 SINGE & PRIME**
***yes*** standard oven singe/HMDS prime

Date _____ Time _____Operator _____

Comments_____

**STEP 5.120- RESIST SPIN COAT**
***svgcoat*** programs 9 (no prime), 7 (coat 1.0 μm of 3612 resist), and 1 (prebake).

System used: ❑***svgcoat*** ❑***svgcoat2***

Date _____ Time _____Operator _____

Comments _____

**STEP 5.140- ALIGNED EXPOSE**
Expose using asml stepper:
Job name: EE410R_1
Layer ID: 6
Layer Number: CONTACT
Image ID: CONTACT
Reticle ID: EE410RET3

Date _____ Time _____ Operator _____

Exposure used:_____

Comments_____

**STEP 5.160 – POST EXPOSURE BAKE**
***svgdev*** programs 9 (no develop) and 1 (bake)

System: ❑***svgdev*** ❑***svgdev2***

Date _____ Time _____Operator _____

Comments_____

**STEP 5.170 RESIST DEVELOP**
Develop using SVG Dev track, programs 3 (develop) and 1 (bake)

System used: ❑***svgdev*** ❑***svgdev2***

Date_____Time _____Operator _____

Comments_____

**STEP 5.180 INSPECTION**
Visual microscope inspection. Check for defects and alignment/exposure quality.

Wafers inspected ____ ____ ____ ____ ____

Date _____ Time _____Operator _____

Comments _____

**STEP 5.190 - POSTBAKE**
Bake in the 110 C postbake oven for 30 minutes.

Date _____ Time _____Operator _____

Comments_____

**REWORK DONE?** ❑***yes*** ❑***no***

Wafers reworked: _____

If yes, attach REWORK sheet here.

## WEEK #5: LAB SECTION

### *20. Oxide Etch*

**STEP 5.200 - POSTBAKE**
Bake in the 110 C postbake oven for 30 minutes.

Date _____ Time _____Operator _____

Comments_____

**STEP 5.220 PLASMA OXIDE ETCH**
Establish the etch rate using T4.

***amtetcher***, Program 3, $CHF_3/O_2$

Etch Time used: _____

Date _____ Time _____Operator _____

Comments_____

**Step 5.240 – STD HARD RESIST STRIP: RESIST ASH**
gasonics, program 013

Date_____ Time _____Operator _____

Comments_____

**STEP 5.260 – STD HARD RESIST STRIP: PIRANHA**
T4 may be removed at this point.

***wbnonmetal***, Piranha @ 120°C, 20', rinse, spin dry

Date_____ Time _____Operator _____

Comments_____

## WEEK #6: PREPARATION

### *21. Metal Deposition*

**STEP 5.300 - STANDARD PRE-DIFFUSION CLEAN**
***wbdiff***, 4:1 H2SO4:H2O2 @ 90°C, 10', rinse;
50:1 DI:HF @ Room Temp, 30 sec, rinse;
5:1:1 DI:H2O2:HCl @ 70°C, 10', rinse, spin dry

Date_____ Time _____Operator _____

Comments_____

***gryphon***, 10,000A of Al/Si
**STEP 5.320 - METAL DEPOSITION**

Date_____ Time _____Operator _____

Comments_____

### *22. PM #6: Metal*

**PHOTOMASK #6 – METAL**
Use T1 and T2 to optimize focus and exposure.

**STEP 6.000 - SINGE & PRIME**
***yes*** standard oven singe/HMDS prime

Date _____ Time _____Operator _____

Comments_____

**STEP 6.120 - RESIST SPIN COAT**
***svgcoat*** programs 9 (no prime), **8** (coat **1.6** μm of 3612 resist), and **2** (prebake).

System used: ❑***svgcoat*** ❑***svgcoat2***

Date _____ Time _____Operator _____

Comments _____

**STEP 6.140 - ALIGNED EXPOSE**
Expose using asml stepper:
Job name: EE410R_1
Layer ID: 4
Layer Number: METAL
Image ID: METAL
Reticle ID: EE410RET2

Date _____ Time _____ Operator _____

Exposure used:_____

Comments_____

**STEP 6.160 – POST EXPOSURE BAKE**
***svgdev*** programs 9 (no develop) and **2** (bake)

System: ❑***svgdev*** ❑***svgdev2***

Date _____ Time _____Operator _____

Comments_____

**STEP 6.170 - RESIST DEVELOP**
Develop using SVG Dev track, programs **4** (develop) and **2** (bake)

System used: ❑***svgdev*** ❑***svgdev2***

Date_____Time _____Operator _____

Comments_____

Visual microscope inspection. Check for defects and alignment/exposure quality.

Wafers inspected ____ ____ ____ ____ ____

Date _____ Time _____Operator _____

Comments _____

**STEP 6.190 - POSTBAKE**
Bake in the 110 C postbake oven for 30 minutes.

Date _____ Time _____Operator _____

Comments_____

**REWORK DONE?** ❑***yes*** ❑***no***

Wafers reworked: _____

If yes, attach REWORK sheet here.

## WEEK #6: LAB SECTION

### *23. Metal Etch*

**STEP 6.200 - POSTBAKE**
Bake in the 110 C postbake oven for 30 minutes.

Date _____ Time _____Operator _____

Comments_____

**STEP 6.210 - METAL ETCH**
***p5000etch***, Recipe CH A. METAL, ~120-150"

Date_____ Time _____Operator _____

Comments_____

**STEP 6.220 - ETCH PASSIVATION**
***wbmetal***, dump-rinser for 6 cycles, spin rinse dry

Date_____ Time _____Operator _____

Comments_____

**Step 6.240 –STD METAL LAYER RESIST STRIP: ASH**
***gasonics***, program 013

Date_____ Time _____Operator _____

Comments_____

## WEEK #6: FINAL PREPARATION

### *24. Anneal/Alloy*

**STEP 6.260 – STD METAL LAYER PRE-FURNACE CLEAN**
Make sure the wafers are dry before putting into bath.

***wbmetal***, PRS1000, @ 40°C, 10', rinse, spin dry

Date_____ Time _____Operator _____

Comments_____

**STEP 6.300 - ANNEAL AND ALLOY**
45' forming gas (4% $H_2$ in $N_2$) @ 400°C

***tylanfga*** Program FGA400

Date_____ Time _____Operator _____

Comments_____

# TEST!

**STEP 100.00 – REWORK SHEET**

**REWORK PHOTOMASK LAYER#** _____

Reworked wafers: _____

**STEP 100.005** ***gasonics***, program 013

Date_____ Time _____Operator _____

Comments_____

**STEP 100.010 - SINGE & PRIME**
***yes*** standard oven singe/HMDS prime

Date _____ Time _____Operator _____

Comments_____

**STEP 100.120 - RESIST SPIN COAT**
❑ Prog 9,7,1 (1μm resist) ❑ Prog 9,8,2 (1.6 μm resist)

System used: ❑***svgcoat*** ❑***svgcoat2***

Date _____ Time _____Operator _____

Comments _____

**STEP 100.140 - ALIGNED EXPOSE**
Expose using ASML Stepper,
❑ 0 – Zero Level: EE410R_1, 0,0,PM,45023981A009
❑ 1 – Active: EE410R_1, 1, ACTIVE, EE410RET1
❑ 2 –PWell: EE410R_1, 2, PWELL, EE410RET1
❑ 3 – Poly: EE410R_1, 3, POLY, EE410RET2
❑ 4 – N-Select: EE410R_1, 5, NSELECT, EE410RET3
❑ 5 – Contact holes: EE410R_1, 6, CONTACT, EE410RET3
❑ 6 – Metal: EE410R_1, 4, METAL, EE410RET2

Date _____ Time _____ Operator _____

Exposure used:_____

Comments_____

**STEP 6.160 – POST EXPOSURE BAKE**
❑ Prog 9,1 (1 μm resist) ❑ Prog 9,2 (1.6 μm resist)

System: ❑***svgdev*** ❑***svgdev2***

Date _____ Time _____Operator _____

Comments_____

**STEP 100.160 - RESIST DEVELOP**
❑ Prog 8,1 (1μm resist) ❑ Prog 4,2 (1.6 μm resist)

System used: ❑***svgdev*** ❑***svgdev2***

Date_____Time _____Operator _____

Comments_____

**STEP 100.180 - INSPECTION**
Visual microscope inspection. Check for defects and alignment/exposure quality.

Date _____ Time _____Operator _____

Comments _____

**STEP 100.00 - REWORK SHEET**

**REWORK PHOTOMASK LAYER#** _____

Reworked wafers: _____

**STEP 100.005** ***gasonics***, program 013

Date_____ Time _____Operator _____

Comments_____

**STEP 100.010 - SINGE & PRIME**
***yes*** standard oven singe/HMDS prime

Date _____ Time _____Operator _____

Comments_____

**STEP 100.120 - RESIST SPIN COAT**
❑ Prog 9,7,1 (1μm resist) ❑ Prog 9,8,2 (1.6 μm resist)

System used: ❑***svgcoat*** ❑***svgcoat2***

Date _____ Time _____Operator _____

Comments _____

**STEP 100.140 - ALIGNED EXPOSE**
Expose using ASML Stepper,
❑ 0 – Zero Level: EE410R_1, 0,0,PM,45023981A009
❑ 1 – Active: EE410R_1, 1, ACTIVE, EE410RET1
❑ 2 –PWell: EE410R_1, 2, PWELL, EE410RET1
❑ 3 – Poly: EE410R_1, 3, POLY, EE410RET2
❑ 4 – N-Select: EE410R_1, 5, NSELECT, EE410RET3
❑ 5 – Contact holes: EE410R_1, 6, CONTACT, EE410RET3
❑ 6 – Metal: EE410R_1, 4, METAL, EE410RET2

Date _____ Time _____ Operator _____

Exposure used:_____

Comments_____

**STEP 6.160 – POST EXPOSURE BAKE**
❑ Prog 9,1 (1 μm resist) ❑ Prog 9,2 (1.6 μm resist)

System: ❑***svgdev*** ❑***svgdev2***

Date _____ Time _____Operator _____

Comments_____

**STEP 100.160 - RESIST DEVELOP**
❑ Prog 8,1 (1μm resist) ❑ Prog 4,2 (1.6 μm resist)

System used: ❑***svgdev*** ❑***svgdev2***

Date_____Time _____Operator _____

Comments_____

**STEP 100.180 - INSPECTION**
Visual microscope inspection. Check for defects and alignment/exposure quality.

Date _____ Time _____Operator _____

Comments _____

**STEP 100.00 - REWORK SHEET**

**REWORK PHOTOMASK LAYER# _____**

Reworked wafers: _____

**STEP 100.005 *gasonics***, program 013

Date_____ Time _____Operator _____

Comments_____

**STEP 100.010 - SINGE & PRIME**
***yes*** standard oven singe/HMDS prime

Date _____ Time _____Operator _____

Comments_____

**STEP 100.120 - RESIST SPIN COAT**
❑ Prog 9,7,1 (1μm resist) ❑ Prog 9,8,2 (1.6 μm resist)

System used: ❑***svgcoat*** ❑***svgcoat2***

Date _____ Time _____Operator _____

Comments _____

**STEP 100.140 - ALIGNED EXPOSE**
Expose using ASML Stepper,
❑ 0 – Zero Level: EE410R_1, 0,0,PM,45023981A009
❑ 1 – Active: EE410R_1, 1, ACTIVE, EE410RET1
❑ 2 –PWell: EE410R_1, 2, PWELL, EE410RET1
❑ 3 – Poly: EE410R_1, 3, POLY, EE410RET2
❑ 4 – N-Select: EE410R_1, 5, NSELECT, EE410RET3
❑ 5 – Contact holes: EE410R_1, 6, CONTACT, EE410RET3
❑ 6 – Metal: EE410R_1, 4, METAL, EE410RET2

Date _____ Time _____ Operator _____

Exposure used:_____

Comments_____

**STEP 6.160 – POST EXPOSURE BAKE**
❑ Prog 9,1 (1 μm resist) ❑ Prog 9,2 (1.6 μm resist)

System: ❑***svgdev*** ❑***svgdev2***

Date _____ Time _____Operator _____

Comments_____

**STEP 100.160 - RESIST DEVELOP**
❑ Prog 8,1 (1μm resist) ❑ Prog 4,2 (1.6 μm resist)

System used: ❑***svgdev*** ❑***svgdev2***

Date_____Time _____Operator _____

Comments_____

**STEP 100.180 - INSPECTION**
Visual microscope inspection. Check for defects and alignment/exposure quality.

Date _____ Time _____Operator _____

**STEP 100.00 - REWORK SHEET**

**REWORK PHOTOMASK LAYER# _____**

Reworked wafers: _____

**STEP 100.005 *gasonics***, program 013

Date_____ Time _____Operator _____

Comments_____

**STEP 100.010 - SINGE & PRIME**
***yes*** standard oven singe/HMDS prime

Date _____ Time _____Operator _____

Comments_____

**STEP 100.120 - RESIST SPIN COAT**
❑ Prog 9,7,1 (1μm resist) ❑ Prog 9,8,2 (1.6 μm resist)

System used: ❑***svgcoat*** ❑***svgcoat2***

Date _____ Time _____Operator _____

Comments _____

**STEP 100.140 - ALIGNED EXPOSE**
Expose using ASML Stepper,
❑ 0 – Zero Level: EE410R_1, 0,0,PM,45023981A009
❑ 1 – Active: EE410R_1, 1, ACTIVE, EE410RET1
❑ 2 –PWell: EE410R_1, 2, PWELL, EE410RET1
❑ 3 – Poly: EE410R_1, 3, POLY, EE410RET2
❑ 4 – N-Select: EE410R_1, 5, NSELECT, EE410RET3
❑ 5 – Contact holes: EE410R_1, 6, CONTACT, EE410RET3
❑ 6 – Metal: EE410R_1, 4, METAL, EE410RET2

Date _____ Time _____ Operator _____

Exposure used:_____

Comments_____

**STEP 6.160 – POST EXPOSURE BAKE**
❑ Prog 9,1 (1 μm resist) ❑ Prog 9,2 (1.6 μm resist)

System: ❑***svgdev*** ❑***svgdev2***

Date _____ Time _____Operator _____

Comments_____

**STEP 100.160 - RESIST DEVELOP**
❑ Prog 8,1 (1μm resist) ❑ Prog 4,2 (1.6 μm resist)

System used: ❑***svgdev*** ❑***svgdev2***

Date_____Time _____Operator _____

Comments_____

**STEP 100.180 - INSPECTION**
Visual microscope inspection. Check for defects and alignment/exposure quality.

Comments _____