

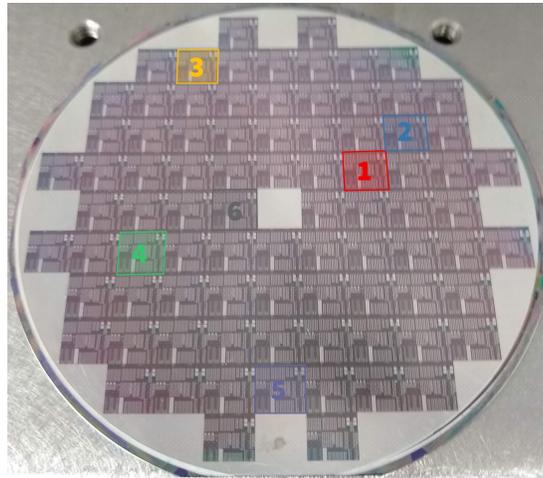
Characteristics of 2019's EE312 process flow using the EE 410 LOCOS Maskset

Yaakov Tuchman

September 29, 2019

Abstract

This report summarizes the typical results obtained with the EE410 LOCOS maskset as outlined in the 2019 EE312 Runsheets (page 10). Herein, we report on the wafer-scale uniformity of device parameters, including performance and materials properties.



Wafer overview with tested dice highlighted in the same color-coded scheme used throughout the report.

Methods

Unless otherwise noted, all measurements in this report were taken at each of the designated dice. All measurements were performed at the **micromanipulator6000** utilizing the attached Keysight B1500A Semiconductor Device Analyzer. Diode and Capacitor measurements were performed with one probe touching the upper surface of the wafer and the other connected to the bottom side of the wafer. Transistor measurements were performed with the body contact held at ground, all transfer curves were taken with $V_D = 0.1V$.

Sheet Resistance

Based on the architecture of the devices, there are only three layers of conductive material: the metal contacts, the n+ silicon active area and the n+ polysilicon gate. Sheet resistance was measured using the 4-point probe and van der Pauw structures in columns p3, p4 and p5 as well as the transmission line structure in p7_1. Overall, the across-wafer variation of sheet resistance seems to be fairly small, with relatively good agreement between measurement methods. Results of the various measurements across each of the dice can be seen in Fig. 1.

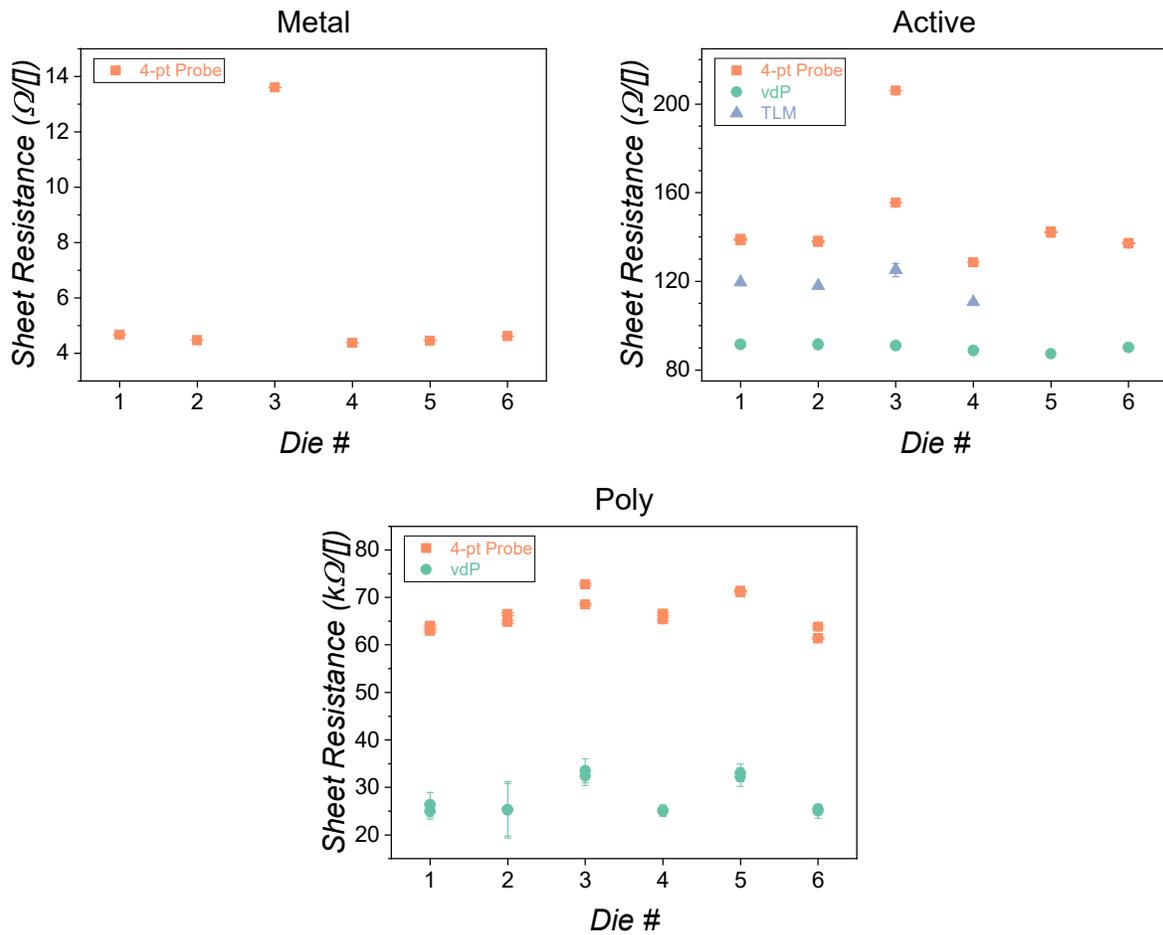


Figure 1: Measured sheet resistance of the metal, active and polysilicon layers, measured via multiple test structures. Notice the relatively good agreement between measurement methods, as well as the uniformity across the measured dice.

Noticeably, the measured sheet resistance of the active layer in Die 3 is also higher, although that may come from an anomalous metal sheet resistance. Another feature worth highlighting is the relatively high polysilicon sheet resistance. As can be seen across the wafer and through multiple measurements, the poly is quite resistive, suggesting some possible issues with the doping process.

Contact Resistance

In measuring and reporting on contact resistance, we focused specifically on the metal to active layer contact both because of the greater number of test features, and because the metal to poly contact resistance was sufficiently high that it could not reliably be extracted using the Kelvin bridge structures. To compare the contact resistance of the active and poly layers, we measured along the contact chain structures p1 & p2, which have taps after 10 and 100 contacts. The calculated resistances were then normalized by number of contacts and plotted in Fig 2. As can be immediately seen from the scales of each figure, the contact resistance associated with the metal to poly contact is several orders of magnitude higher than to the active layer. While the contact chain measurement *does* include some contribution from sheet resistance, the contribution should be on the order of $200\text{ k}\Omega$, which does not account for the majority of the measured contact resistance. Additionally, the further increase in normalized resistance per contact for the longer contact chain indicates a significant Schottky contact, given the lower field present in the 100-contact case. On the other hand, the active layer seems to exhibit fairly low and consistent resistances over the course of the contact chain structure. The slight increase in resistance may be attributable to a variety of factors, but the overall values are consistent with the sheet resistance values measured above, allowing a viable exploration of the areal dependence of the contact resistance.

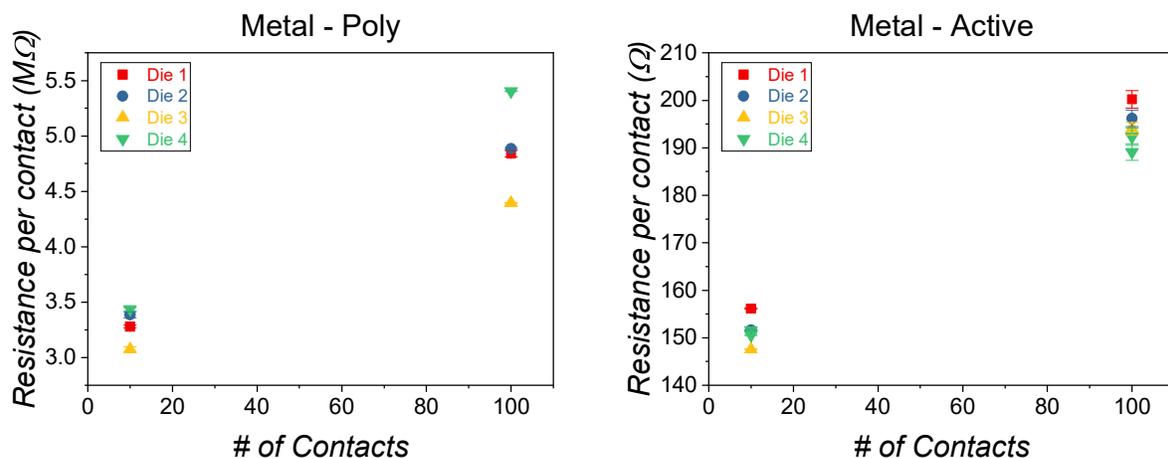


Figure 2: Calculated resistance per contact from the contact chain structure. Measurements are normalized by number of contacts traversed.

Utilizing the Kelvin bridge structures in p6, we calculate the contact resistance for contact holes with areas of $\{2\mu\text{m}^2, 2.25\mu\text{m}^2, 4\mu\text{m}^2 \text{ \& } 16\mu\text{m}^2\}$ and plot contact resistance normalized to contact area in Fig. 3. For the larger contacts, the values seem to be fairly consistent across size and across the wafer, although they begin to diverge at the $2.25\mu\text{m}^2$ point, with only Die #1 maintaining consistent contact down to $1\mu\text{m}^2$. Practically, though all of the actual devices in the layout utilize $2\mu\text{m} \times 2\mu\text{m}$ contact holes with an area of $4\mu\text{m}^2$, so while the smaller contact holes may be more resistive, we do not expect that to impact device performance whatsoever. Indeed, we can compare the contact resistance

measured directly with the Kelvin bridge structures to that of the transmission line structure p7_1, which uses the same $4\mu\text{m}^2$ contact holes. After properly normalizing to area, we find on the right side of Fig. 3 that the extracted contact resistance measured through TLM qualitatively agrees with the Kelvin bridge measurement, although the relative precision of the TLM measurement is significantly worse. The diversion of the TLM data from the Kelvin bridge measurement seems to be slightly correlated with radial distance from the center, although it is difficult to imagine a justification for such a correlation. More likely, the large error in Die #3 is a result of the higher sheet resistance of both the active and metal layers on that die, and/or correlated to whatever led to those higher sheet resistances.

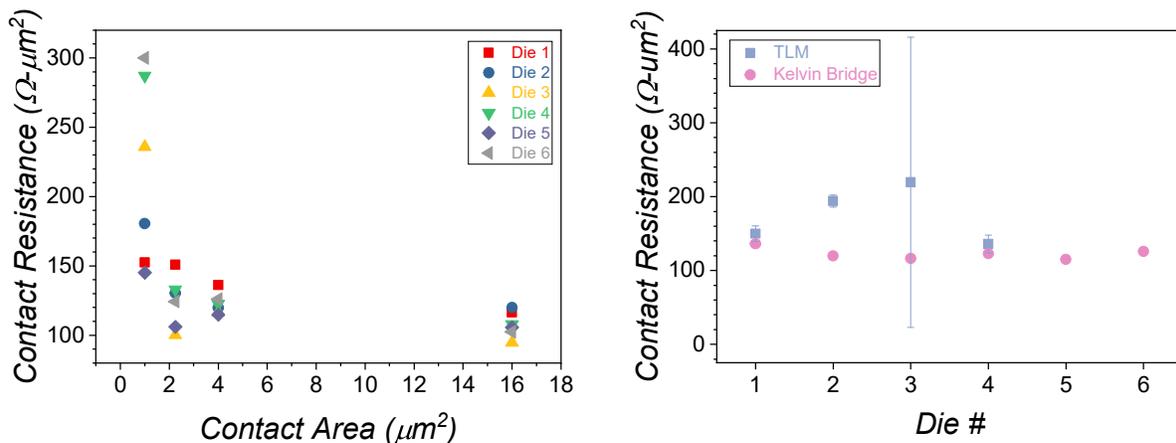


Figure 3: LEFT: Contact resistance as a function of contact area using a Kelvin bridge structure. RIGHT: Comparison of transmission line contact resistance with the equivalent data from the $4\mu\text{m}^2$ Kelvin bridge structure.

Oxide Thickness

The three oxide thicknesses that are relevant to the process are the gate oxide, field oxide and the LTO oxide meant for encapsulation. Throughout the fabrication process, various oxide thickness are measured optically using the *nanospec* ellipsometer using specially designed test structures. In addition to in-line measurements, the oxide thickness can also be probed electrically by measuring the capacitance of the MOS capacitors that straddle each of the various oxide layers. When the capacitance is measured in the accumulation regime, (+3V in our case, see Fig. 4a) the resulting oxide thickness can easily be calculated. From the equation describing a capacitor, the thickness of the oxide is:

$$x_{ox} = \frac{\kappa_{ox}\epsilon_0 A}{C_{ox}}$$

where the dielectric constant of SiO_2 , $\kappa_{ox} = 3.9$ and the permittivity of free space, $\epsilon_0 = 8.85 \times 10^{-14} \text{F/cm}$. The simulated, measured, and calculated oxide thicknesses across the wafer at the various dice are summarized in Fig. 4b-d.

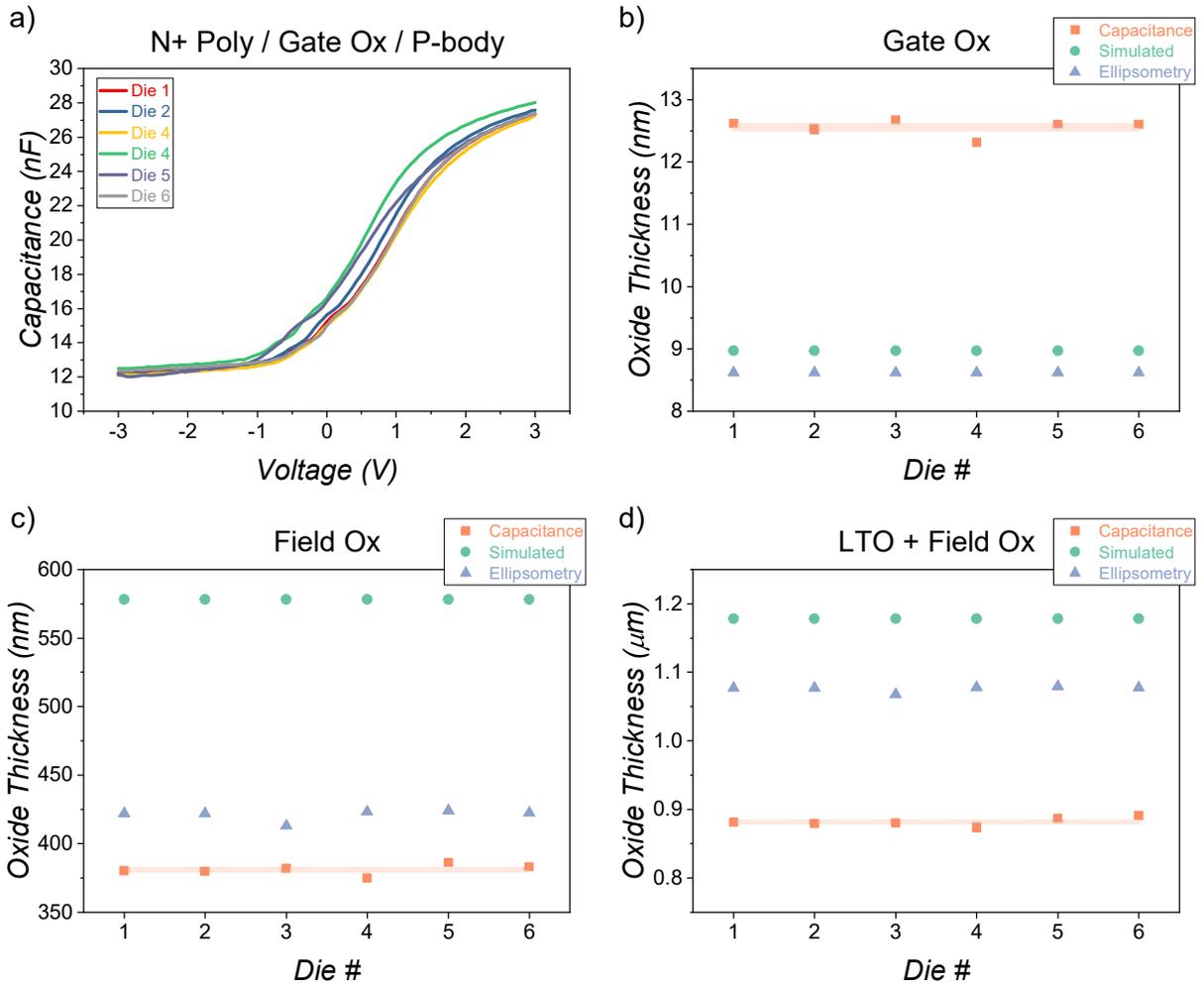


Figure 4: (a) Capacitance of the gate oxide capacitor *d11_4* as a function of bias voltage for each of the measured dice. Oxide thickness comparison from the accumulation mode capacitance, SENTAURUS simulation and in-line ellipsometry for the (b) gate oxide, (c) field oxide and (d) LTO + field oxide, with the standard deviation from the mean denoted using a shaded rectangle in the background.

Diode Behavior

Ideal PN diode behavior should follow the current-voltage relationship given by:

$$I = I_0 \left(e^{\frac{V}{n} \frac{q}{kT}} - 1 \right)$$

with $\frac{q}{kt} = 38.76 \text{mV}^{-1}$, applied voltage V , reverse saturation current I_0 , and ideality factor n . An examination of the I-V curves from across the wafer in Fig. 5 reveals normal characteristics, with a breakdown voltage around -5V . Fitting the exponential behavior in the region from $+0.3$ to $+0.7$ to the equation given above for an ideal diode allows for

extraction of approximate values for the ideality factor and reverse saturation current for each die. The slightly lower values seen in Die 5 *may* indicate slightly poorer doping near the flat, although there is insufficient evidence to strongly support such a hypothesis, especially due to the rather unremarkable characteristics of Die 3 (near the top). Thus, it is probably more likely that the relative fluctuations in values were result of other issues than non-uniform doping.

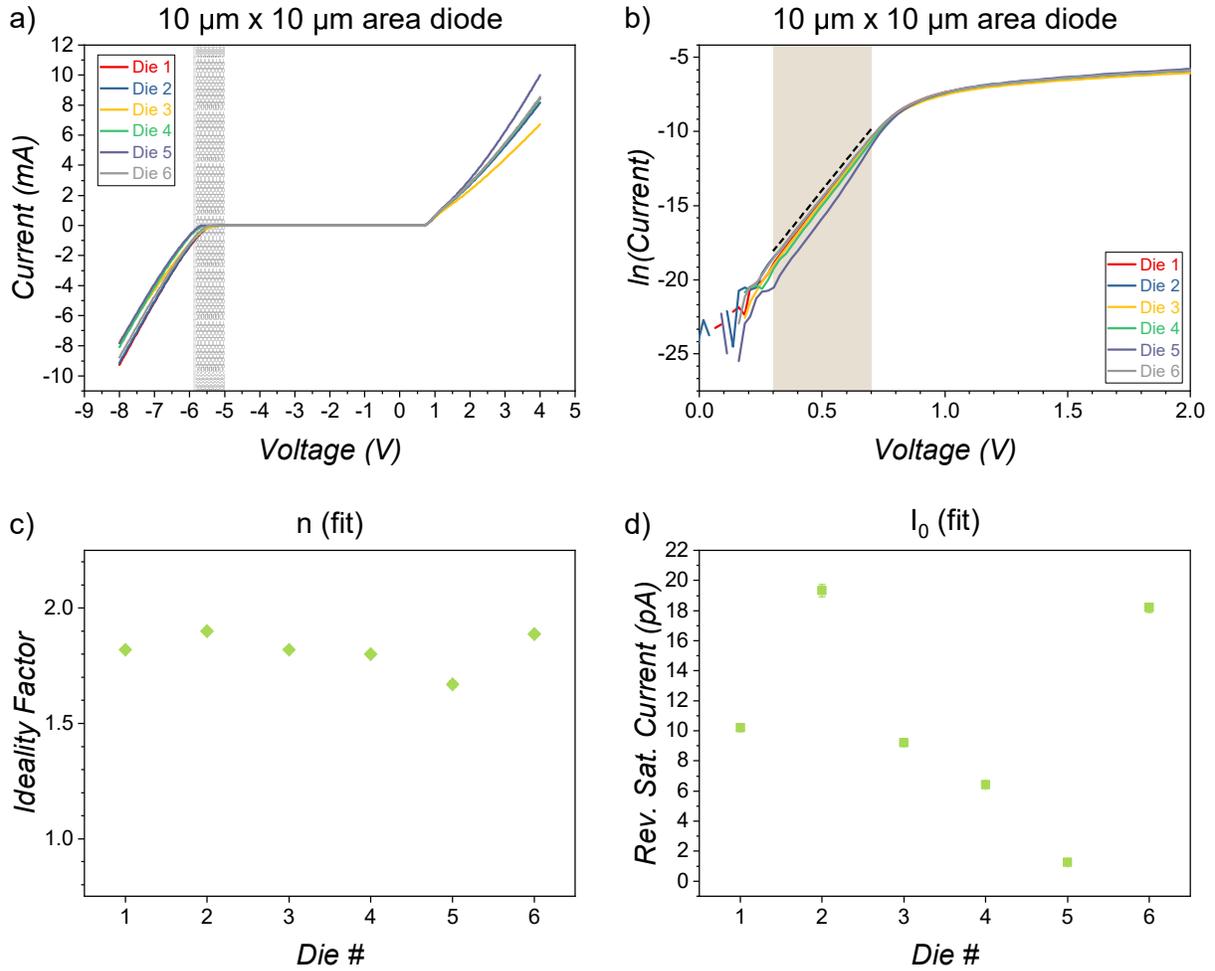


Figure 5: (a) I-V characteristics of diode D12_3 on each of the measured dice. Note the breakdown voltage denoted by the grey crosshatched background at approximately -5V . (b) Log-scale inset of the same I-V curves, highlighting the region of exponential growth from which the (c) ideality factor and (d) reverse saturation current were calculated.

NMOS Transistor Characteristics

The NMOS transistors present in the layout include several series of devices. Here, we study the performance of devices with constant channel width and varying channel length (d1 and d2) as well as the series with constant channel length and varying channel width (d3). We do not examine the minimum feature series (d4), though the devices are available should the interested reader intend to pursue such measurements.

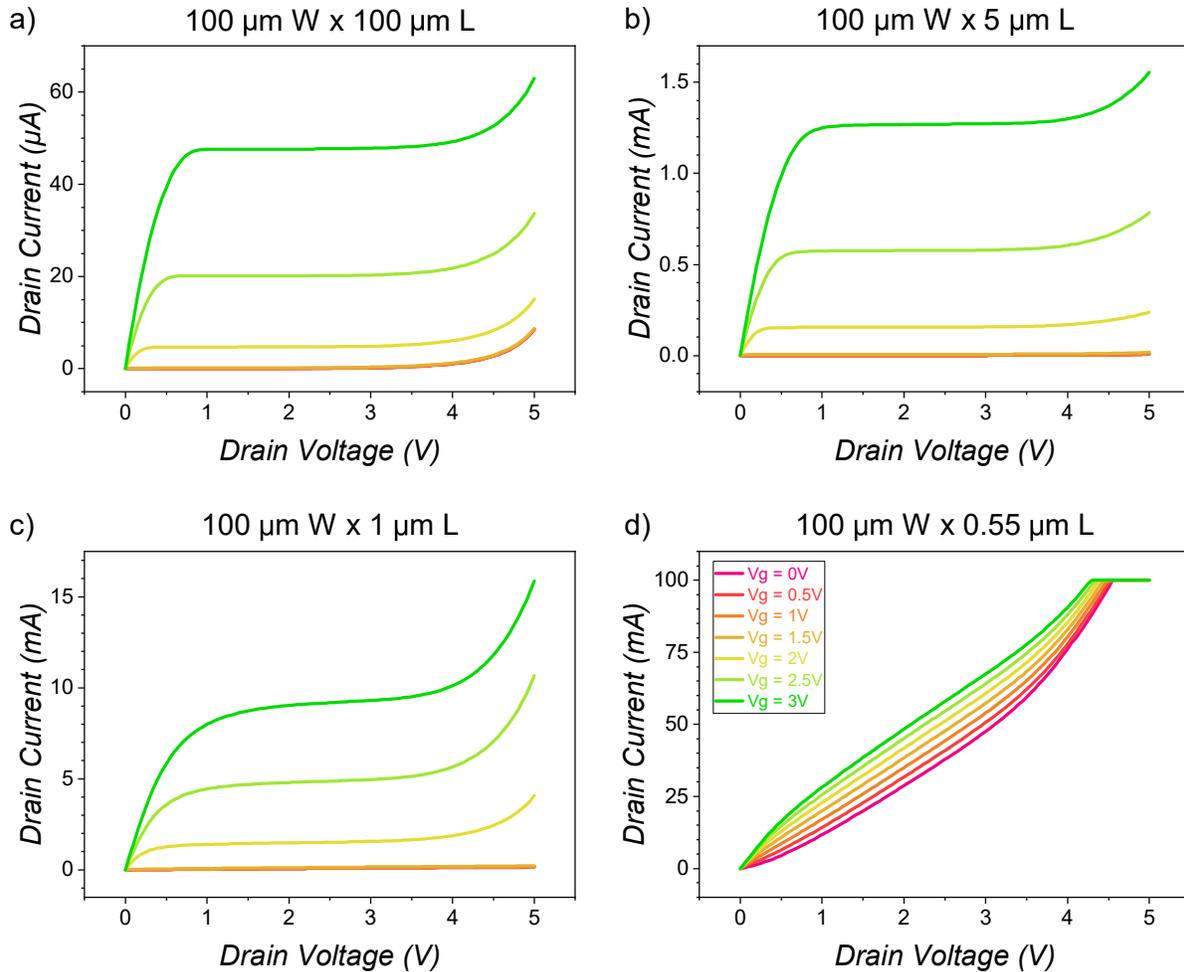


Figure 6: Output curves of various devices in the d1 and d2 sets of transistors on Die #2. The legend in (d) is common across all four graphs.

Beginning with the channel length series, the sets of d1 & d2 contain 10 transistors, all with width of $100\mu\text{m}$ and channel length varying across the range of $\{100\mu\text{m}, 25\mu\text{m}, 5\mu\text{m}, 2.5\mu\text{m}, 1\mu\text{m}, 0.75\mu\text{m}, 0.6\mu\text{m}, 0.55\mu\text{m}, 0.5\mu\text{m}, 0.45\mu\text{m}\}$. As can be seen from the output curves in Fig. 6 taken from the transistors on Die 2, as the channel length shrinks, the devices exhibit mildly increasing non-ideality, which can most readily be seen in the saturation regime. Firstly, as the devices get smaller, the drain current does not stay flat

throughout the saturation regime, with the gradual increase in voltage getting progressively worse with decreasing channel length. Additionally, the while the spacing between curves should go quadratically with the gate voltage, that trend clearly begins to deviate with the $1\mu m$ device. Additionally, as can be seen from Fig. 6d, below a certain dimension, the devices cease to function entirely.

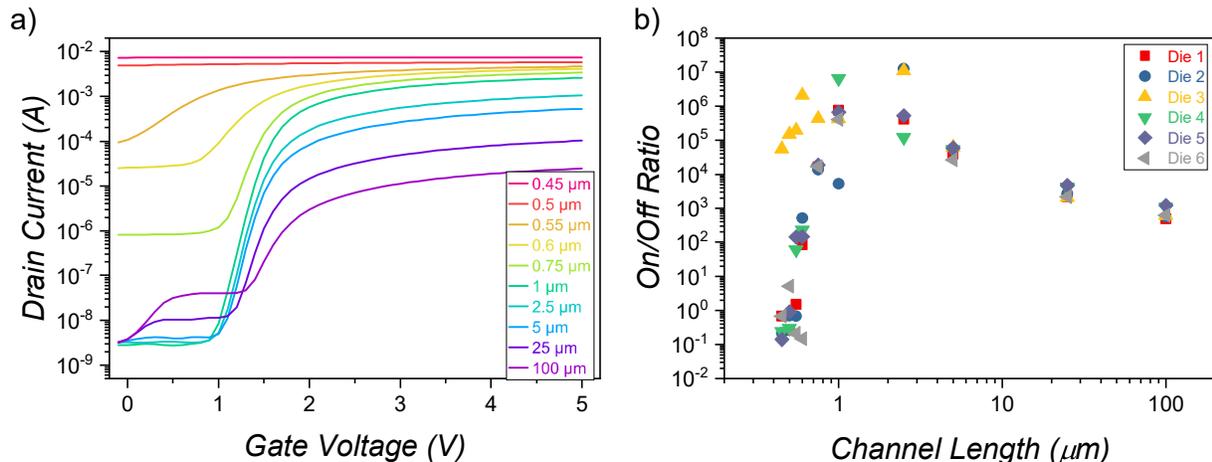


Figure 7: (a) Transfer curves of the d1 and d2 sets of transistors on Die #1, with constant width of $100\mu m$ and variable channel length. (b) Across-wafer comparison of the On/Off ratio for the same series of transistors, measured at $0V$ and $+5V$.

To examine the length scale below which the devices would no longer operate as expected, we plotted a series of transfer curves for all of the devices on a single die, and used the same information to extract the On/Off ratio as a function of channel length in Fig. 7. As the channel length shrinks, the on/off ratio initially increases as expected because of the increased field for sweeping out charge without introducing short channel effects. However, as the devices pass the $1\mu m$ threshold, the on/off ratios begin to fall dramatically, with virtually no modulation present, similar to the output curve in Fig. 6d.

In addition to analyzing the on/off ratio, we also examined the effect of both length and width on the threshold voltage. In order to extract the threshold voltage from a given transfer curve, a linear extrapolation was made from the point of maximum transconductance to intersect with magnitude of the off current, as shown in Fig. 8a. Although such calculations could be performed manually, in this report, we chose to utilize the automated calculation within the Keysight software.

The similar trend described in Fig. 7 regarding the degradation of devices below the $1\mu m$ channel length is evident as well in both the calculated threshold voltage (Fig. 8b, which remains relatively flat with channel length before sharply diving around $1\mu m$, as well as in the maximum transconductance g_m which increases in magnitude significantly due to the expected scaling of the drain current in the linear regime given by

$$I_D = \mu C_{ox} \frac{W}{L} (V_G - V_T) V_D$$

However, as the channel length shrinks below approximately $1\mu m$, the transconductance drops off steeply due to the disappearance of the channel. It is particularly remarkable

that across all of the metrics of on/off ratio, threshold voltage and maximum transconductance, the devices on Die 3 still seem to function nominally even at the shortest channel lengths, especially given the fact that other than a higher metal sheet resistance, there didn't seem to be anything out of the ordinary about that particular die.

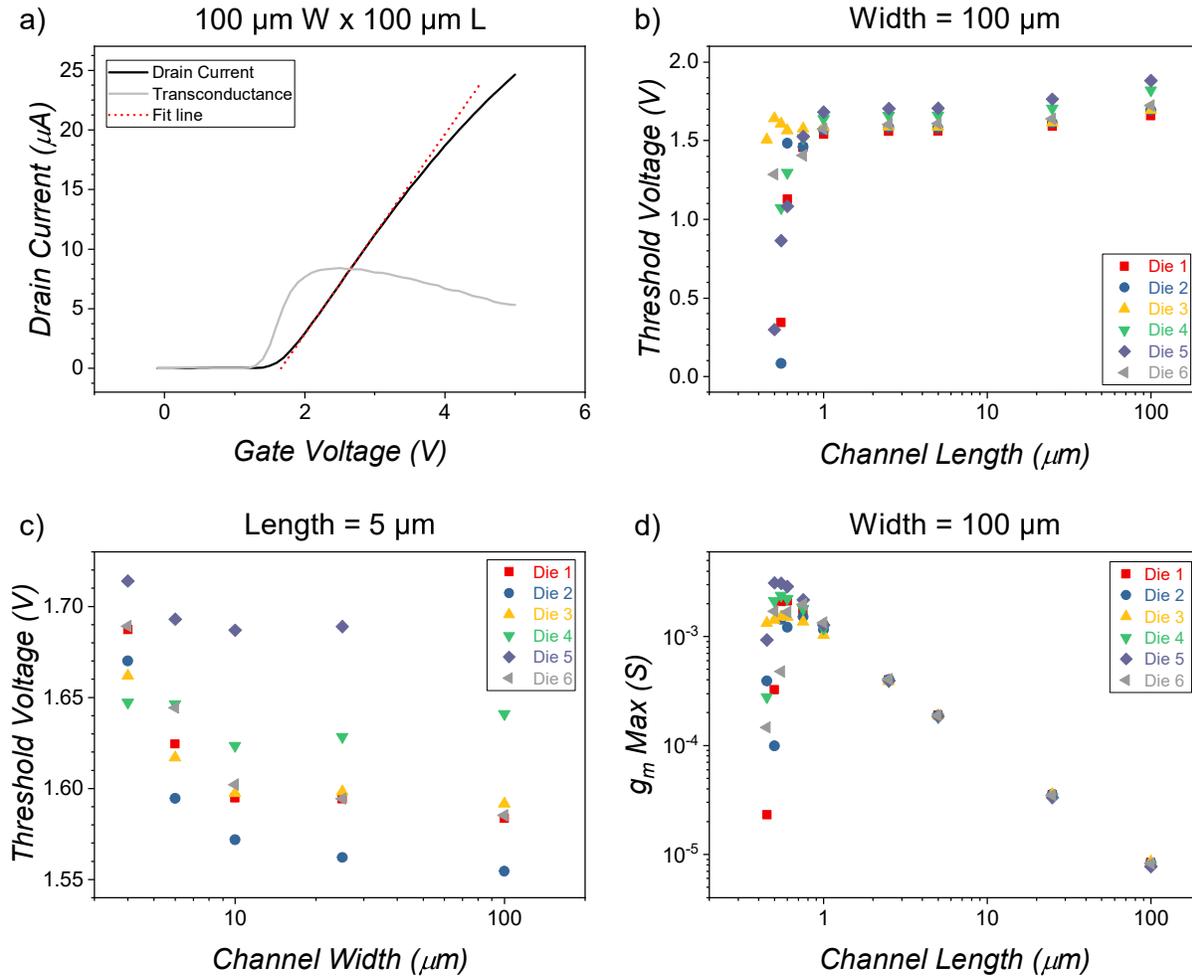


Figure 8: (a) Transfer curve of the $d1_1$ transistor from Die 1 with the transconductance shown in grey and the fit line for threshold voltage calculation shown in red. (b) Change in threshold voltage as a function of channel length and (c) channel width. (d) Effect of channel length on peak transconductance.

Lastly, we examine the effect of maintaining a constant channel length at $5\ \mu\text{m}$ and varying the width, as shown in Fig. 8c. As expected, the threshold voltage increased slightly with narrower channels, although the variation in threshold voltage across the wafer seems to be of greater magnitude than the effect seen by narrowing the channel.

STEP 0.00 - PHOTOMASK #0- ZERO LEVEL MARKS

Starting material: P-type silicon:
12X - (5-10 ohm-cm?) - K-Prime
12X - (10-20 ohm-cm?) - L-Prime

Add 9 test wafers labeled as follows:

- T1-3: Implant test wafers
T4: oxide deposition test wafer, will be added to all oxidation steps through field oxide to monitor thickness
T5: nitride deposition test wafer, added to nitride deposition only to confirm thickness
T6: Gate oxide test wafer, added to gate oxidation and LTO steps
T7: Poly test wafer, standard 1000A oxide
TR: Travels with Resist implant protected wafers and gets all processing steps except implant
TO: Travels with Oxide implant protected wafers and gets all processing steps except implant

STEP 0.01 - SCRIBE & CLEAN

All wafers
Hand-scribe wafers on the front side near the flat. Angle the lettering so no lines are drawn perpendicular or parallel to the flat.

Piranha Clean in wbclean_res-piranha - 120°C; 10min; Dump rinse; SRD

Date Time Operator

STEP 0.10 - SINGE & PRIME

All device wafers plus TR & TO
yes standard oven singe/HMDS prime

Date Time Operator

Comments

STEP 0.12 - SPIN COAT RESIST (Use svgcoat2)

All device wafers plus TR & TO
Apply 1 micron of 3612 positive resist w/o VP and 2mm Edge Exclusion, using SVG Coat track programs 7 (coat and softbake).

System used: svgcoat2 svgcoat (backup option)

Date Time Operator

Comments

STEP 0.14 - Spin Rinse Dry - LithoSRD

All device wafers plus TR and TO; Inspect backside of wafers for particles/ resist, clean w/ q-tip if needed prior to SRD

Date Time Operator

Comments

STEP 0.20 - NON-ALIGNED EXPOSURE - ASML stepper:

Job name: ee410LOCOSR1
Layer ID: GLOBALMARKS Layer Number: 0
Image ID: XPA Reticle ID: 45023981A009

Exposure used: 70mJ

Date Time Operator

Comments

STEP 0.30 - POST EXPOSE BAKE

Bake using SVG Dev track, bake program 1 (bake only)

System used: svgdev svgdev2

Date Time Operator

Comments

STEP 0.35 - RESIST DEVELOP

Develop using SVG Dev track, develop program 3 (develop) and bake program 1 (bake)

System used: svgdev svgdev2

Date Time Operator

Comments

STEP 0.40 - VISUAL INSPECTION

Visual microscope inspection. Check for defects, alignment and exposure quality.

Wafers inspected

Date Time Operator

Comments

REWORK DONE? yes no

Wafers reworked:

If yes, attach REWORK sheet here.

STEP 0.50 - ALIGNMENT MARK SILICON ETCH

All device wafers plus TR & TO
Target step height 1200A+/-200A

amtetcher, Program 4 for 5 - 6min or lampoly, Recipe: Zero_Mark_Etch, 10s BT+20s ME (adjust etch time to target)

System: amtetcher lampoly

Date Time Operator

Comments

STEP 0.60 - RESIST ASH

All device wafers plus TR & TO

gasonics, recipe sequence 014

Date Time Operator

Comments

STEP 0.70 - STANDARD RESIST STRIP

All device wafers plus TR & TO

Wbclean_res_piranha, Piranha @ 120°C, 30', dump rinse, spin dry

Date Time Operator

Measure step ht (Spec 1200+/-200A)

Comments

STEP 1.0 - BLANKET BORON IMPLANT -Vt Adjust (Optional)
 All device wafers- Add one bare Si (K-Prime) TW (T1) per box (scribed w/ implant ID) for monitoring; Store test wafers after implant.) - B₁₁⁺ - 4E13/cm²; 100keV; 7 deg tilt
Implant Facility: *Luxience*

Species/Dose/ Energy/Tilt _____

Date _____ Time _____ Operator _____

Comments _____

STEP 1.01 – Post Implant Sulfuric Clean
 All device wafers plus T1.

Wbclean_res_piranha, Piranha @ 120°C, 30', dump rinse, spin dry

Date _____ Time _____ Operator _____

Comments _____

STEP 1.05 - STANDARD PRE-DIFFUSION CLEAN
 All device wafers plus T4, T5, TR, TO

Wbclean-1 or -2, 5:1:1 H₂O:H₂O₂:NH₄OH, 50°C, 10', dump rinse, 50:1 DI:HF @ Room Temp, 30 sec, dump rinse 5:1:1 DI:H₂O₂:HCl @ 50°C, 10', dump rinse, spin dry

Date _____ Time _____ Operator _____

Comments _____

STEP 1.1 - LOCOS PAD OXIDATION GROWTH
 All device wafers plus T4, TR, TO.

Wet Oxide at 850°C, for 12min., ≈ 200Å,

Thermco3: 3WETOX Tube Used: _____

Date _____ Time _____ Operator _____

Oxide Growth Time: _____

Comments: _____

STEP 1.2 - LOCOS NITRIDE DEPOSITION
 All device wafers plus T5, TR, TO @ 785°C, 2,000 Å
 Wafers must go In to Nitride deposition within 1 hour of oxide growth.

thermcoNitride1: Program: N2 Tube used _____

Nitride Deposition Time: _____

Date _____ Time _____ Operator _____

Comments: _____

STEP01.25 –THICKNESS MEASUREMENT
 Use Woollam, WVASE program EE410 / LOCOS to measure the oxide and nitride thickness and uniformity on T1.

Oxide: T _____ C _____ B _____ R _____ L _____

Nitride: T _____ C _____ B _____ R _____ L _____

Thk % Uniformity: Oxide _____ Nitride _____

Comments _____

STEP 1.3 – IMPLANT PROTECT OXIDE DEPOSITION
 K1-6, L1-6, TO. 350C, 3000A

Ccpdep **Recipe:** SiO350-0

Date _____ Time _____ Operator _____

Deposition Time: _____

Thicness Measurement on TW _____

Comments: _____

STEP 2.00 - PHOTOMASK #1- ISO
 All device wafers plus TO. Use TO to optimize focus and exposure.

STEP 2.10 - SINGE & PRIME
yes standard oven singe/HMDS prime

Date _____ Time _____ Operator _____

Comments _____

STEP 2.12 - SPIN COAT RESIST
 Apply 1 micron of 3612 positive resist w/o VP and 2mm Edge Exclusion, using SVG Coat track programs 7 (coat and softbake).

System used: **svgcoat2** **svgcoat (backup option)**

Date _____ Time _____ Operator _____

Comments _____

STEP 2.14 – Spin Rinse Dry -All device wafers plus TO
 Inspect & clean backside of all wafers for particles/ resist residue

LithoSRD

Date _____ Time _____ Operator _____

Comments _____

STEP 2.00 - PHOTOMASK #1- ISO
 All device wafers plus TO. Use TO to optimize focus and exposure.

STEP 2.10 - SINGE & PRIME
yes standard oven singe/HMDS prime

Date _____ Time _____ Operator _____

Comments _____

STEP 2.12 - SPIN COAT RESIST
 Apply 1 micron of 3612 positive resist w/o VP and 2mm Edge Exclusion, using SVG Coat track programs 7 (coat and softbake).

System used: **svgcoat2** **svgcoat (backup option)**

Date _____ Time _____ Operator _____

Comments _____

STEP 2.14 – Spin Rinse Dry -All device wafers plus TO
 Inspect & clean backside of all wafers for particles/ resist residue

LithoSRD

Date _____ Time _____ Operator _____

Comments _____

REWORK DONE? yes no

Wafers reworked: _____
 If yes, attach REWORK sheet here.

STEP 2.2 – ALIGNEDFOCUS-EXPOSURE MATRIX
 Expose using ASML stepper:
 Job name: ee410LOCOSR1
 Layer ID: 1 Layer Number: ISO
 Image ID: ISO Reticle ID: EE410 2008 1

Focus Minimum: 0.0 um Focus Step: 0.2 um

Exposure Min: **40mJ** (do not go any lower) Exposure Step: 10 mJ

Focus Used: _____ Exposure Used: _____

Date _____ Time _____ Operator _____

Comments _____

STEP 2.5– OXIDE + LOCOS NITRIDE DRY ETCH
 All device wafers plus TO. Use TO for etch set up.

P5000 Ch. B - Modify Ch.B Oxide to endpoint after oxide and nitride etches and add Ch.B Nit-Spacer conditions for overetch

Etch Time ME/OE _____

Date _____ Time _____ Operator _____

Comments _____

STEP 2.22 - ALIGNED EXPOSURE
 Expose using ASML stepper:
 Job name: ee410LOCOSR1
 Layer ID: 1 Layer Number: ISO
 Image ID: ISO Reticle ID: EE410 2008 1

Focus Used: _____ Exposure used: _____

Date _____ Time _____ Operator _____

Comments _____

STEP 2.55 - THICKNESS MEASUREMENT
 Use Nanospec program 7. Measure Pad oxide thickness on TO.

Oxide: T _____ C _____ B _____ R _____ L _____

Thk % Uniformity: Oxide _____

Comments _____

STEP 2.25 – POST EXPOSE BAKE
 Bake using SVG Dev track, bake program 1 (bake only)

System: svgdev svgdev2

Date _____ Time _____ Operator _____

Comments _____

STEP 2.6 - RESIST ASH
 All device wafers plus TO
gasonics, recipe sequence 014

Date _____ Time _____ Operator _____

Comments _____

STEP 2.3 - RESIST DEVELOP
 Develop using SVG Dev track, develop program 3 (develop) and bake program 1 (bake)

System: svgdev svgdev2

Date _____ Time _____ Operator _____

Comments _____

STEP 2.65 - STANDARD RESIST STRIP
 All device wafers plus TO

Wbclean_res-piranha, Piranha@120°C, 20', dump rinse,spin dry

Date _____ Time _____ Operator _____

Comments _____

STEP 2.4 – VISUAL INSPECTION
 Visual and microscope inspection. Check for defects, alignment and exposure quality.

Wafers inspected _____

Date _____ Time _____ Operator _____

Comments _____

STEP 2.7 – P+ Isolation Implant

All device wafers- Add one bare Si TW per box (TL2) -scribed w/ implant ID) for monitoring; Store test wafers after implant.

Luxience: B₁₁⁺ -1E15/cm2; 30keV; 7 deg tilt.

Date _____ Time _____ Operator _____

Comments _____

STEP 2.75 – POST IMPLANT SULFURIC CLEAN
 All device wafers plus TO

Wbclean_res_piranha, Piranha @ 120°C, 30', dump rinse, spin dry

Date _____ Time _____ Operator _____

Comments _____

STEP 2.78 – MASKING OXIDE WET STRIP
 All device wafers plus TO to remove PECVD oxide on top of LOCOS nitride
 Use T4 to establish etch rate.

Wbclean_res-hf, 20:1 BOE Etch, dump rinse, spin dry

Etch Time: _____

Date _____ Time _____ Operator _____

Comments _____

STEP 2.79 - STANDARD PRE-DIFFUSION CLEAN
 All device wafers plus T4, TR, TO

Wbclean-1 or -2, 5:1:1 H2O:H2O2:NH4OH, 50°C, 10', dump rinse, 50:1 DI:HF @ Room Temp, 30 sec, dump rinse 5:1:1 DI:H2O2:HCl @ 50°C, 10', dump rinse, spin dry

Date _____ Time _____ Operator _____

Comments _____

STEP 2.8 - FIELD OXIDATION
 All device wafers plus T4, TR, TO. Ramped process

Wet Oxide at 1000C, 1hr:40 min, ~5,400 Å

Thermco3: 3WETOX

Date _____ Time _____ Operator _____

Comments _____

STEP 2.82 – THICKNESS MEASUREMENT
 Use Nanospec program 1 to measure the Field oxide thickness and uniformity on TR/TO.

Oxide: T _____ C _____ B _____ R _____ L _____

Thk % Uniformity: Oxide _____

Comments _____

STEP 2.85 – OXIDIZED NITRIDE STRIP
 All device wafers plus TR, TO in 6:1 BOE, ~45sec.

Wbclean_res-hf

Etch Time: _____

Date _____ Time _____ Operator _____

Comments: _____

STEP 2.90 – NITRIDE WET STRIP
 All device wafers plus TR, TO.

Wbclean_res-hotphos, Hot Phosphoric Acid, 155C, ~85min. , dump rinse, spin dry

Etch Time: _____

Date _____ Time _____ Operator _____

Comments: _____

STEP 2.92 – THICKNESS MEASUREMENT
 Use Nanospec program 1 to measure the field oxide and program 7 to measure the Pad oxide and uniformity on TR/TO.

FieldOx: T _____ C _____ B _____ R _____ L _____

Thk % Uniformity: FieldOx _____

PadOx: T _____ C _____ B _____ R _____ L _____

Thk % Uniformity: PadOx _____

Comments _____

STEP 2.93 - STANDARD PRE-DIFFUSION CLEAN
 All device wafers plus T6, TR, TO

Wbclean-1 or -2, 5:1:1 H2O:H2O2:NH4OH, 50°C, 10', dump rinse, 50:1 DI:HF @ Room Temp, 30 sec, dump rinse 5:1:1 DI:H2O2:HCl @ 50°C, 10', dump rinse, spin dry

Date _____ Time _____ Operator _____

Comments _____

STEP 2.95 – Kooi Oxidation and Drive-In
 All device wafers plus T6, TR, TO

Wet Oxide at 850C, 15min

Thermco3: 3WETOX

Date _____ Time _____ Operator _____

Comments _____

STEP 2.98 – THICKNESS MEASUREMENT
 Use the Nanospec program 1 to measure the Kooi oxide thickness and uniformity on TR/TO.

Oxide: T _____ C _____ B _____ R _____ L _____

Thk % Uniformity: Oxide _____

Comments _____

STEP 3.0 - STANDARD PRE-DIFFUSION CLEAN
 All device wafers plus T6, T7, TR, TO

Wbclean-1 or -2, 5:1:1 H2O:H2O2:NH4OH, 50°C, 10', dump rinse; 50:1 DI:HF @ Room Temp, 30 sec, dump rinse; 5:1:1 DI:H2O2:HCl @ 50°C, 10', dump rinse, spin dry

Date _____ Time _____ Operator _____

Comments _____

STEP 3.05 – SACRIFICIAL (KOOI) OXIDE STRIP
 All device wafers plus T6, TR, TO

Wbclean-1 or -2 50:1 DI:HF @ Room Temp, dump rinse, spin dry

Etch Time: _____ mins

Date _____ Time _____ Operator _____

Comments _____

STEP 3.10 - THICKNESS MEASUREMENT

Use Nanospec program 7 (thin oxide) to measure TR/TO to ensure complete Sacrificial oxide removal.

System used: nanospec nanospec2

T _____ C _____ B _____ R _____ L _____

Date _____ Time _____ Operator _____

Comments _____

STEP 3.15 - GATE OXIDATION

All device wafers plus T6, TR, TO.

Dry Oxide at 900C: 20 min, ~100Å

NOTE: Run TLCCLEA program on Thermco 1/3 to clean tube before gate oxidation. This will take about 4 hours to complete.

Tube used: Thermco1 Thermco3
1TLCCLEA 3TLCCLEA
1DRYOX 3DRYOX

Oxidation Time: _____

Date _____ Time _____ Operator _____

Comments: _____

STEP 3.2 - POLYSILICON DEPOSITION

All device wafers plus T7, TR, TO. T6 has been removed for Gate Ox measurement.

LPCVD @ 550°C, ≈ 2,000Å

NOTE: Wafers must go immediately into thermcopoly after GateOx with no cleaning steps. This is to ensure contamination is minimal.

Thermcopoly Program P550POLY

Deposition Time: _____

Date _____ Time _____ Operator _____

Comments: _____

STEP 3.25 – THICKNESS MEASUREMENT

Use Woollam, WVASE program EE410 / GATE POLY to measure the oxide and nitride thickness and uniformity on TR/TO.

Poly: T _____ C _____ B _____ R _____ L _____

Oxide: T _____ C _____ B _____ R _____ L _____

Thk % Uniformity: Poly _____ Oxide _____

Comments _____

STEP 3.30 - PHOTOMASK #2 - GATE

All device wafers plus TR & TO. Use TR/TO to optimize focus and exposure

STEP 3.30 - SINGE & PRIME

yes standard oven singe/HMDS prime

Date _____ Time _____ Operator _____

Comments _____

STEP 3.32 - SPIN COAT RESIST

Apply 1 micron of 3612 positive resist w/o VP and 2mm Edge Exclusion, using SVG Coat track programs 7 (coat and softbake). System used: svgcoat2 svgcoat (backup option)

Date _____ Time _____ Operator _____

Comments _____

STEP 3.34 – Spin Rinse Dry -All device wafers plus T1 and T2
Inspect and clean backside of wafers for particles/ resist residues
LithoSRD

Date _____ Time _____ Operator _____

Comments _____

STEP 3.39 – ALIGNED FOCUS-EXPOSURE MATRIX

Expose using ASML stepper:

Job name: ee410LOCOSR1

Layer ID: GATE

Image ID: GATE

Layer Number: 3

Reticle ID: EE410 2008 1

Focus: 0.2 um, step of 0.

Exposure Min: **40mJ** (do not go any lower) Exposure Step: 10 mJ

Focus Used: _____ Exposure Used: _____

Date _____ Time _____ Operator _____

Comments _____

STEP 3.4 – ALIGNED EXPOSE

Expose using asml stepper:

Job name: ee410LOCOSR1

Layer ID: GATE

Image ID: GATE

Layer Number: 3

Reticle ID: EE410 2008 1

Date _____ Time _____ Operator _____

Exposure used: _____

Comments _____

STEP 3.42 – POST EXPOSE BAKE

Bake using SVG Dev track, bake program 1 (bake only)

System: svgdev svgdev2

Date _____ Time _____ Operator _____

Comments _____

STEP 3.45- RESIST DEVELOP

Develop using SVG Dev track, develop program 3 (develop) and bake program 1 (bake)

System used: svgdev svgdev2

Date _____ Time _____ Operator _____

Comments _____

STEP 3.50 - INSPECTION

Inspect and clean backside of all wafers for particles/ residues. Visual and microscope inspection. Check for defects, alignment AND exposure quality.

Wafers inspected _____

Date _____ Time _____ Operator _____

Comments _____

REWORK DONE? yes no

Wafers reworked: _____
If yes, attach REWORK sheet here.

STEP 3.6 - POLY ETCH

All device wafers plus T7 and TR/TO to verify end point.

P5000 Ch. C Program: Ch.C POLY ETCH End Point Algorithm: SU_POLY1.alg; Backup: **lampoly**, Recipe: Poly_Etch_endpoint

System used: P5000 lampoly

Etch Time ME/OE _____

Date _____ Time _____ Operator _____

Comments _____

STEP 3.65- RESIST ASH

All device wafers plus TR/TO

gasonics, recipe sequence 014

Date _____ Time _____ Operator _____

Comments _____

STEP 3.68 - STANDARD RESIST STRIP

All device wafers plus TR/TO

Wbclean_res-piranha, Piranha @ 120°C, 20', dump rinse, SRD

Date _____ Time _____ Operator _____

Comments _____

STEP 3.7 - POLYMER SIDEWALL STRIP

All device wafers plus TR/TO

Wbclean_res-hf, 50:1 HF Dip, Dump rinse, SRD

Etch Time: _____

Date _____ Time _____ Operator _____

Comments _____

STEP 3.8 - N-SOURCE/DRAIN IMPLANT (Blanket implant)

All device wafers - Add one bare Si TW per box (TL3) scribed w/ implant ID for monitoring; Store test wafers after implant.

Luxience: 50 keV, As75, $2 \times 10^{15} \text{ cm}^{-2}$

Date _____ Time _____ Operator _____

Comments _____

STEP 3.85 - Post Implant Clean

All device wafers plus TR/TO

Wbclean_res-piranha, Piranha @ 120°C, 20', dump rinse, SRD

Date _____ Time _____ Operator _____

Comments _____

STEP 3.9 - STANDARD PRE-DIFFUSION CLEAN

All device wafers plus T6, TR and TO.

Wbclean-1 or -2, 5:1:1 H₂O:H₂O₂:NH₄OH @ 50°C, 10', dump rinse; 50:1 DI:HF @ Room Temp, 30 sec, dump rinse; 5:1:1 DI:H₂O₂:HCl @ 50°C, 10', dump rinse, spin dry

Date _____ Time _____ Operator _____

Comments _____

STEP 4.0 - LTO DEPOSITION

All device wafers plus T6, TR and TO (for LTO measurement after Densification).

Undoped LPCVD @ 400°C, ≈ 6000Å

tylanbpsg, Program LTO400PC

Deposition Time: _____

Date _____ Time _____ Operator _____

Comments _____

STEP 4.05 - MODIFIED PRE-DIFFUSION CLEAN

All device wafers plus T6, TR and TO (for LTO measurement after Densification).

Note: The Modified Pre-Diffusion clean may be omitted if wafers move from LTO dep to LTO densification in less than one hour.

Wbclean-1 or -2, 5:1:1 H₂O:H₂O₂:NH₄OH @ 50°C, 10', dump rinse; 5:1:1 DI:H₂O₂:HCl @ 50°C, 10', dump rinse, spin dry

Date _____ Time _____ Operator _____

Comments _____

STEP 4.1 - LTO DENSIFICATION

All device wafers plus T6, TR and TO

Wet Oxide @ 950C, 30' min

Tube used: Thermco1 1WETOX Thermco3 3WETOX

Date _____ Time _____ Operator _____

Comments _____

STEP 4.15 - THICKNESS MEASUREMENT

Use Nanospec program 1 to measure the LTO thickness and uniformity on TR/TO.

Oxide: T _____ C _____ B _____ R _____ L _____

Thk % Uniformity: Oxide _____

Comments _____

STEP 4.20 - PHOTOMASK #3 - CONTACT
All device wafers plus T6, TR and TO.
Use TR/TO to optimize focus and exposure.
T6 will be an etch test wafer and so needs to be patterned.

STEP 4.22 - SINGE & PRIME
yes standard oven singe/HMDS prime
Date _____ Time _____ Operator _____
Comments _____

STEP 4.24 - SPIN COAT RESIST
Apply 1 micron of 3612 positive resist w/o VP and 2mm Edge Exclusion, using SVG Coat track programs 7 (coat and softbake).
System used: **svgcoat2** **svgcoat (backup option)**
Date _____ Time _____ Operator _____
Comments _____

STEP 4.26 - Spin Rinse Dry- All device wafers plus T1 and T2
Inspect and clean backside for particles and resist residues
LithoSRD
Date _____ Time _____ Operator _____
Comments _____

STEP 4.29 - ALIGNED FOCUS-EXPOSURE MATRIX
Expose using ASML stepper:
Job name: ee410LOCOSR1
Layer ID: CONTACT Layer Number: 6
Image ID: CONTACT Reticle ID: EE410 2008 2
Focus: 0.2 um, step of 0.
Exposure Min: **40mJ** (do not go any lower) Exposure Step: 10 mJ
Focus Used: _____ Exposure Used: _____
Date _____ Time _____ Operator _____
Comments _____

STEP 4.3- ALIGNED EXPOSE
Expose using asml stepper:
Job name: ee410LOCOSR1
Layer ID: CONTACT Layer Number: 6
Image ID: CONTACT Reticle ID: EE410 2008 2
Date _____ Time _____ Operator _____
Exposure used: _____
Comments _____

STEP 4.35 - POST EXPOSE BAKE
Bake using SVG Dev track, bake program 1 (bake only)
System: **svgdev** **svgdev2**
Date _____ Time _____ Operator _____
Comments _____

STEP 4.4- RESIST DEVELOP
Bake using SVG Dev track, programs 3 (develop) and 1 (bake)
System used: **svgdev** **svgdev2**
Date _____ Time _____ Operator _____
Comments _____

STEP 4.45 - VISUAL INSPECTION
Visual and microscope inspection. Check for defects, alignment and exposure quality.
Wafers inspected _____
Date _____ Time _____ Operator _____
Comments _____

REWORK DONE? **yes** **no**
Wafers reworked: _____
If yes, attach REWORK sheet here.

STEP 4.5- PLASMA OXIDE ETCH
All device wafers plus T6, TR and TO. Establish the etch rate using TR/TO. - Etch time to include 30% overetch
Amtetcher - Program 3, CHF₃/O₂
P5000 - Ch. B Oxide
System used: **P5000** **amtetcher**
Etch Time ME/OE _____
Date _____ Time _____ Operator _____
Comments _____

STEP 4.55 - THICKNESS MEASUREMENT
Use Nanospec program 7 (thin oxide) to measure TR/TO to ensure complete oxide removal.
System used: **nanospec** **nanospec2**
T _____ C _____ B _____ R _____ L _____
Date _____ Time _____ Operator _____
Comments _____

STEP 4.55 - RESIST ASH
All device wafers plus T6, TR/TO
gasonics, recipe sequence 014
Date _____ Time _____ Operator _____
Comments _____

STEP 4.6 STANDARD RESIST STRIP
All device wafers plus T6, TR/TO
Wbclean_res-piranha, Piranha @ 120°C, 20', rinse, SRD
Date _____ Time _____ Operator _____
Comments _____

STEP 4.7- STANDARD PRE-METAL CLEAN

All device wafers plus TR/TO

Wbclean-1 or-2, 5:1:1 H2O:H2O2:NH4OH @ 50°C, 10', dump rinse; 5:1:1 DI:H2O2:HCl @ 50°C, 10', dump rinse 50:1 DI:HF @ Room Temp, 30 sec, dump rinse; spin dry

Date _____ Time _____ Operator _____

Comments _____

STEP 5.00 - METAL DEPOSITION – GOLD CONTAMINATED

Lesker_sputter,

Sputter clean off surface oxide

50 A Ti

200 A TiN

6000 A of Al-1%Si

Date _____ Time _____ Operator _____

Comments _____

STEP 5.10 - PHOTOMASK #4 - METAL

All device wafers

STEP 5.12 - SINGE & PRIME

yes standard oven singe/HMDS prime

Date _____ Time _____ Operator _____

Comments _____

STEP 5.14 -1.6 micron SPIN COAT RESIST

Apply 1.6 micron of 3612 positive resist w/o VP and 2mm Edge Exclusion, using SVG Coat track program 8 (coat and softbake).

System used: : **svgcoat2** **svgcoat (backup option)**

Date _____ Time _____ Operator _____

Comments _____

STEP 5.16 – Spin Rinse Dry

Inspect and clean backside for particles and resist residues

LithoSRD

Date _____ Time _____ Operator _____

Comments _____

STEP 5.2 - ALIGNED EXPOSE

Expose using asml stepper:

Job name: ee410LOCOSR1

Layer ID: METAL Layer Number: 7

Image ID: METAL1 Reticle ID: EE410 2008 2

Date _____ Time _____ Operator _____

Exposure used: _____

Comments _____

STEP 5.25 – POST EXPOSE BAKE

Bake using SVG Dev track, bake program 2 (bake only)

System: **svgdev** **svgdev2**

Date _____ Time _____ Operator _____

Comments _____

STEP 5.3 - RESIST DEVELOP

Bake using SVG Dev track, programs 4 (develop) and 2 (bake)

System used: **svgdev** **svgdev2**

Date _____ Time _____ Operator _____

Comments _____

STEP 5.35 – VISUAL INSPECTION

Inspect and clean backside for particles and resist residues

Visual and microscope inspection. Check for defects, alignment and exposure quality.

Wafers inspected _____

Date _____ Time _____ Operator _____

Comments _____

REWORK DONE?

yes

no

Wafers reworked: _____

If yes, attach REWORK sheet here.

STEP 5.40 - METAL ETCH

PT-MTL; Recipe: Al_HiSel_Std ~ 60 sec

Etch Time ME/OE _____

Date _____ Time _____ Operator _____

Comments _____

STEP 5.45 – POST ETCH METAL RINSE

Must be done immediately following removal from etch system

Wbmetal-gold, dump rinse, spin rinse dry

Date _____ Time _____ Operator _____

Comments _____

STEP 5.5 - METAL RESIST STRIP

Make sure the wafers are dry before putting in to SRS-100 bath.

Wbmetal-gold, SRS-100,@ 60°C, 20'; dump rinse, spin dry

Date _____ Time _____ Operator _____

Comments _____

STEP 5.6 - METAL CLEAN

Make sure the wafers are dry before putting in to PRS1000 bath.

Wbmetal-gold PRS1000,@ 40°C, 10', dump rinse, spin dry

Date _____ Time _____ Operator _____

Comments _____

STEP 5.6 - ANNEAL AND ALLOY
 45 min forming gas (4% H₂ in N₂) @ 400°C?

Tylan9 Program 400FGA

Date _____ Time _____ Operator _____

Comments _____

STEP 6.0 – BACKSIDE REMOVAL – GOLD CONTAMINATED

STEP 6.1 - SINGE & PRIME
yes standard oven singe/HMDS prime

Date _____ Time _____ Operator _____

Comments _____

STEP 6.2 -1.6 micron SPIN COAT RESIST
 Apply 1.6 micron of 3612 positive resist w/o VP & NO EBR, using SVG Coat track program 8 (coat and softbake).

System used: : *svgcoat2* *svgcoat (backup option)*

Date _____ Time _____ Operator _____

Comments _____

STEP 6.3 – RESIST HARDENING BAKE
 Bake using SVG Dev track, bake program 2 (bake only)

System: *svgdev* *svgdev2*

Date _____ Time _____ Operator _____

Comments _____

STEP 6.3 – BACKSIDE LTO STRIP
 Use T6 to establish etch rate.

Wbflexcorr 1-2 or 3-4, 6:1 BOE Etch, ~ 4.5 min
 Rinse in beaker, spin dry

Etch Time: _____

Date _____ Time _____ Operator _____

Comments _____

STEP 6.3 – BACKSIDE POLY PLASMA ETCH
 Use T6 to establish etch rate.

Drytek2, poly etch, ~2 min

Etch Time: _____

Date _____ Time _____ Operator _____

Comments _____

STEP 6.3 – BACKSIDE METAL DEPOSITION

Aja-evap, Al or Ti deposition: 2000-4000 A

Thickness: _____

Date _____ Time _____ Operator _____

Comments _____

STEP 100.00 - REWORK SHEET
REWORK PHOTOMASK LAYER# _____

Reworked wafers: _____

Resist removal for wafers before metal deposition:

wbnonmetal, piranha clean, dump rinse 6X, spin-rinse dry

Date _____ Time _____ Operator _____

Resist removal for wafers after metal deposition

wbmetal, PRS1000, dump rinse, spin-rinse dry

Date _____ Time _____ Operator _____

Comments _____

STEP 100.18 - VISUAL INSPECTION

Visual and microscope inspection. Check for defects, alignment and exposure quality.

Wafers inspected _____

Date _____ Time _____ Operator _____

Comments _____

STEP 100.10 - SINGE & PRIME

yes standard oven singe/HMDS prime

Date _____ Time _____ Operator _____

Comments _____

STEP 100.12 - RESIST SPIN COAT

Apply 1 micron of 3612 positive resist w/o VP and 2mm Edge Exclusion, using SVG coat programs 7 (coat and softbake)

System used: : **svgcoat2** **svgcoat (backup option)**

Date _____ Time _____ Operator _____

Comments _____

STEP 100.13 – Spin Rinse Dry- All device wafers plus T1 and T2 - Inspect and clean backside for particles and resist residues

LithoSRD

Date _____ **Time** _____ **Operator** _____

Comments _____

STEP 100.14 - ALIGNED EXPOSE

Expose using ASML Stepper,

0 – Global Marks: ee410LOCOSR1: 45023981A009

1 – ISO: ee410LOCOSR1: EE410 2008 1

2 – Gate: ee410LOCOSR1: EE410 2008 1

3 – Contact: ee410LOCOSR1: EE410 2008 2

4 – Metal: ee410LOCOSR1: EE410 2008 2

Exposure Used: _____

Date _____ Time _____ Operator _____

Comments _____

STEP 100.16 - RESIST DEVELOP

Develop using SVG Dev track, programs 3 (develop) and 1 (bake)

System used: **svgdev** **svgdev2**

Date _____ Time _____ Operator _____

Comments _____