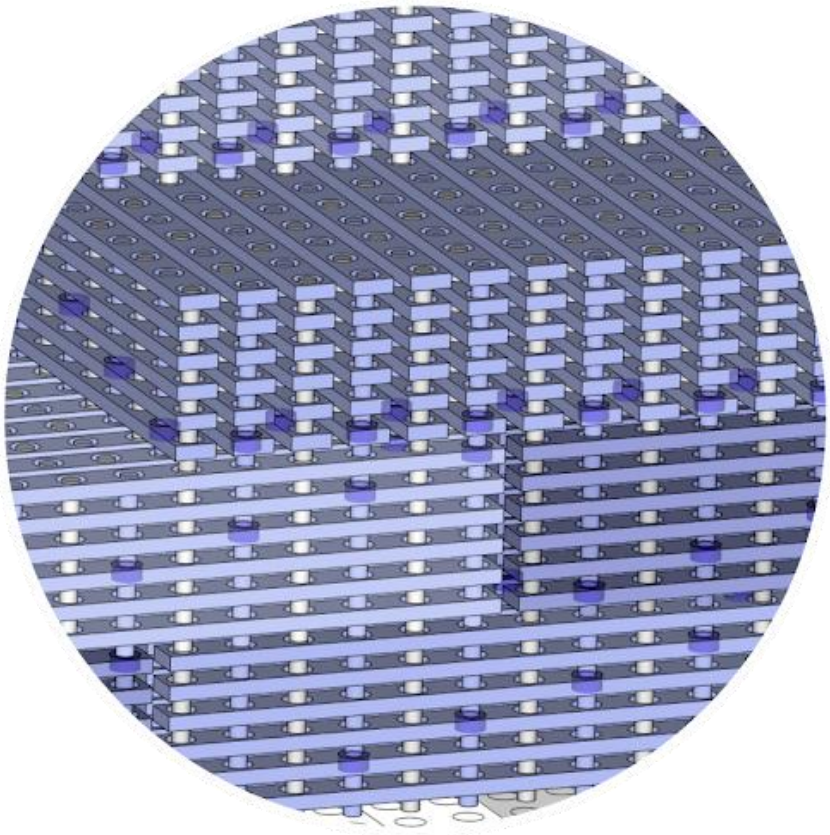

E241 Final Report:

Fabrication of cylindrical antifuse for cost-efficient 3D ICs

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E241 Spring 2025

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1. Introduction

1.1. Motivation

As silicon nodes grow more costly and complex with limited performance gains, and data demands surge, a fundamental shift in chip design is needed. One promising direction is transitioning from the current 2D processes, all logic and memory in a single layer, into 3D. Over the past decade, 3D chips have gained significant appeal from their ability to increase transistor density [1] and on-chip memory [2], and allow for previously impossible architectural optimization [3]. Despite this, the technology has been slow to market. Die-stacking approaches, using through-silicon vias or hybrid bonding, [4] remain limited by alignment accuracy and process throughput, while monolithic 3D, fabricating multiple layers on a single chip [5], requires additional mask steps for every added layer, increasing process complexity and decreasing potential yield.

One potential solution for this high process complexity has been introduced in 3D NAND flash in the form of the bit-cost scalable (BiCS) fabrication process, decoupling the number of layers from the number of required process steps [6]. 3D NAND (Fig. 1) is currently being used BiCS commercially and could be a source for process improvements in the logic design space. A possible building block for scalable 3D logic with hundreds of layers is a one-time programmable cylindrical antifuse (Fig. 2). By taking advantage of high-voltage breakdown conditions, the cylindrical antifuse allows a pass-through vertical via to be connected to a unique horizontal wire without requiring lithography at each level.

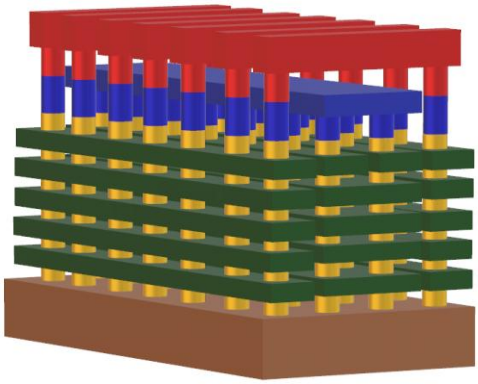

Fig. 1: 3D NAND Structure design by Akihiro Nitayama et. al. [6] We recreated to demonstrate the 3D crossbar and via structure utilized by 3D NAND.

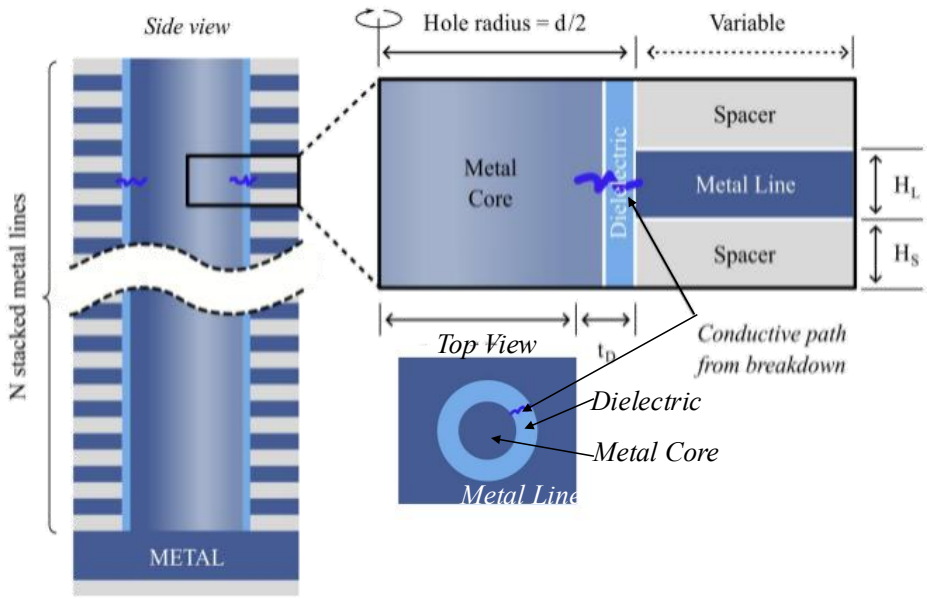

Fig. 2: Cylindrical Antifuse design across N stacked metal layers. Selective connection occurs at a single metal line using breakdown across the dielectric.

The cylindrical antifuse could be integrated into a bit-cost scalable 3D NAND process flow with minimal modification. Past antifuse breakdown conditions and resistivity measurements have only been done in planar designs, [7]. This presents us with a unique test case for E241: designing and fabricating a cylindrical antifuse to verify its functionality.

1.2. Summary of work performed

In this class we focus on fabricating a single layer of antifuses using optical lithography. Following existing literature, we develop our process (Fig. 3) for a metal-insulator-metal stack made from tungsten, aluminum oxide, and titanium nitride. We then characterize the antifuse breakdown (Fig. 4), including its pre and post breakdown resistance and the breakdown voltage.

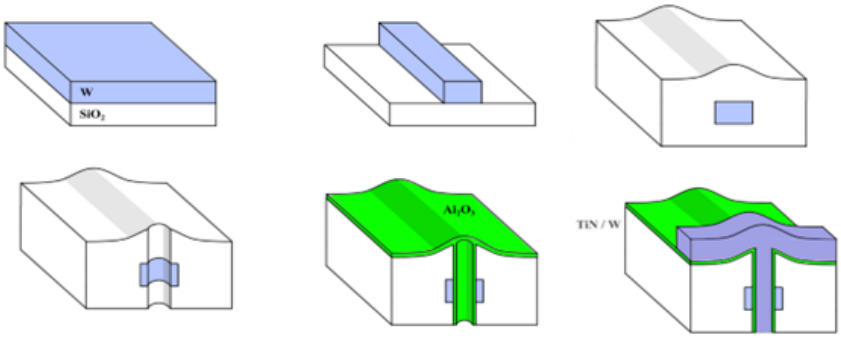

Fig. 3: Visually depicting the antifuse process flow. We design a 6-step process flow to fabricate the antifuse as described in detail in our process flow.

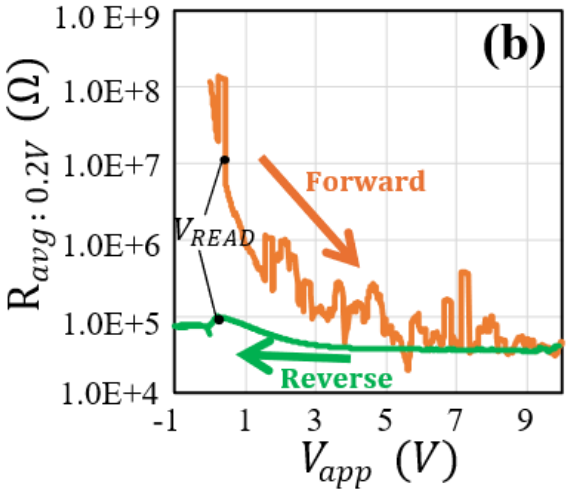

Fig. 4: Forward and Reverse voltage sweep for antifuse breakdown and resistance measurement. This measurement captures the change in resistance from before to after breakdown.

1.3. Benefits to the SNF community

Exploring low-mask alternatives for complex wiring benefits the SNF community in two ways.

1.3.1. Cylindrical Antifuses

Cylindrical antifuses allow for a simple method to implement more complex, multi-layer wiring in projects without drastically increasing the project complexity or mask count. This work has demonstrated the capability of a metal and cylindrical Al_2O_3 antifuse, and when combined with the new deep etching equipment and improved atomic layer deposition (ALD), can be expanded into more complex designs.

1.3.2. Process characterization

In our work we implemented several processes which have not been previously explored in depth in the SNF. as detailed further in the standard operating procedures (SOP), such processes include:

- Aluminum oxide hard masks for HF vapor etching
- Dry etching titanium and titanium nitride while protecting an underlying tungsten layer

2. Design, fabrication, and measurement

2.1. Test chip design

Our chip is designed with multiple antifuse and wire sizes, in addition to three metal-short tests to verify continuity of metal structures after etching, and to measure the metal resistivity to compare against the final antifuse measurements, depicted in Fig. 5.

Given the limitation of the Heidleberg2's accuracy to within 900nm, the antifuses range in diameter of 1 µm to 8 µm, as specified in

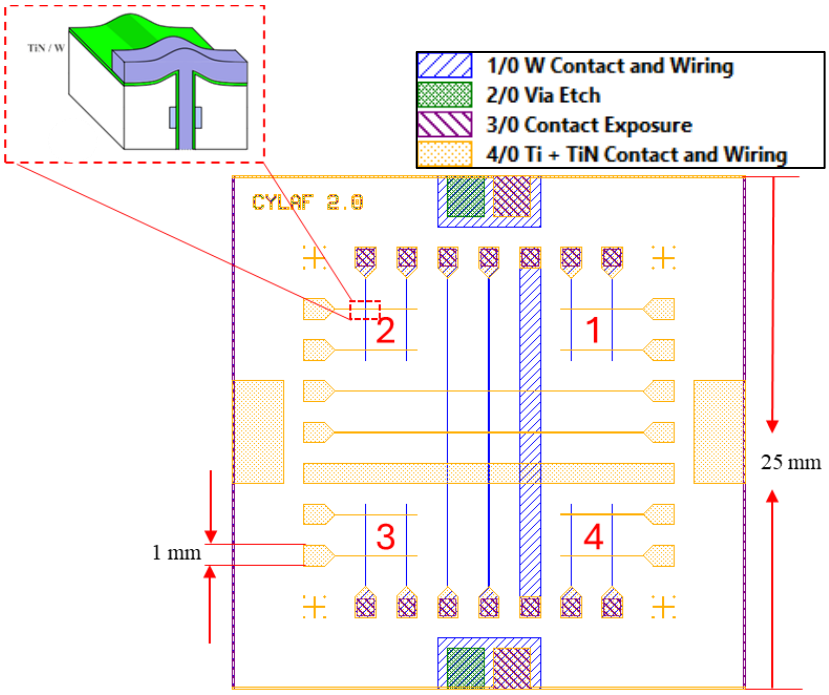

Fig. 5: 25 mm chip design for cylindrical antifuse testing. Antifuses are defined in the numbered quadrants, with expected patterning highlighted near 2. Antifuse dimensions are further detailed in Table 1. Central short-tests are defined to measure metal resistance to determine resistivity and to ensure the minimum wire width (1.8 µm) is not over etched.

Quadrant	*Wire W*	*Hole D*
1	1.8 µm	1 µm
2	3.6 µm	2 µm
3	7.2 µm	4 µm
4	14.4 µm	8 µm

Table 1: Wire width and hole diameter. Defined for each specified quadrant in Fig. 5. Hole diameter and wire width scaling allow for tests on process reliability and changes in on/off ratio with scaled features.

2.2. Cylindrical antifuse fabrication

Based on existing literature, we fabricate our antifuse as a metal-insulator-metal (MIM) stack using tungsten, aluminum oxide, and titanium nitride. Additional titanium is added to increase contact thickness.

- **W outer electrode**: A planar study [7] showed that a 400 nm CVD-W bottom layer works and survives the breakdown pulse; we kept it for its low resistivity, high melting point. It is relatively inert (compared to Ti used for the inner electrode) and commonly used for deep trench and via fill.
- **ALD Al_2O_3 dielectric**: Conformal, high-κ, rich in oxygen-vacancy traps—exactly the ingredients Tian et al. linked to repeatable hard breakdown and very low Ron. The thickness of this layer is the object of a **process split** to better characterize its impact on breakdown.
- **Ti vs TiN/Ti inner electrode:** Ti scavenges oxygen, giving ≈1.2 V lower breakdown voltage than TiN; TiN is more inert and narrows the distribution. A thin TiN barrier plus Ti cap lets us dial the programming window for our 3D cylindrical antifuse without new process steps.

2.2.1. Tungsten contact and wires

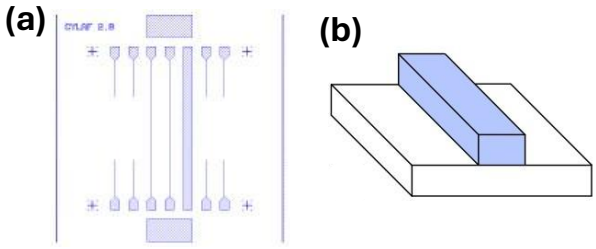

Fig. 6: Tungsten contacts and wires "mask 1" (a) and 3D structure (b).

To fabricate the tungsten contacts and wires (fig 6), we deposit 20 nm of tungsten, followed by a patterning and dry etch (fig 7).

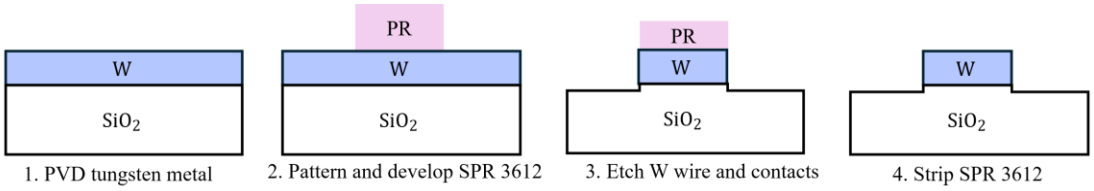

Fig. 7: Tungsten layer process flow. Blanket sputter and etched pattern from mask 1 to define tungsten contacts and wires.

The tungsten is sputtered using DC magnetron sputtering on the Lesker 2 in conditions defined by Table 2.

Deposition	DC
Power	200 W
Pressure	5 mTorr
Duration	210s
Thickness	20-30 nm (profilometer)

Table 2: Tungsten sputter conditions. Used deposit 20 nm of tungsten for bottom wires and contacts.

The target deposition conditions, and duration were first characterized using long deposition times (10 minutes) both on lesker 1 and lesker 2 on dummy wafers. The thickness of deposited tungsten was estimated by masking a portion of the chip using Kapton tape during deposition to create a step and measuring the step height with the Alphastep 500 profilometer (alphastep).

For our actual wafer, the thickness of the deposited tungsten after 3 min 30s was also measured and estimated to be in the range ~20-30 nm, with a margin of uncertainty linked to the profilometer limited resolution for such thin steps.

We then pattern the desired contacts and wires from mask 1 (Fig 6), using Shipley 3612 (SPR 3612) resist and the Heidelberg MLA 150 – 2 (heidelberg2). The pattern is then developed using MF26A developer. The SOP for this process is described in detail in Appendix 2.

Using PT-MTL, recipe *W_SF6_N2_SWF1_bias* (Table 5), we etch for 100 seconds, ~20-30 nm of tungsten and ~17-27 nm of SiO_2. After stripping the photoresist, the pattern was optically inspected, shown in Fig. 8, and the resistance of the metal shorts are measured to determine approximate resistivity (Table 3).

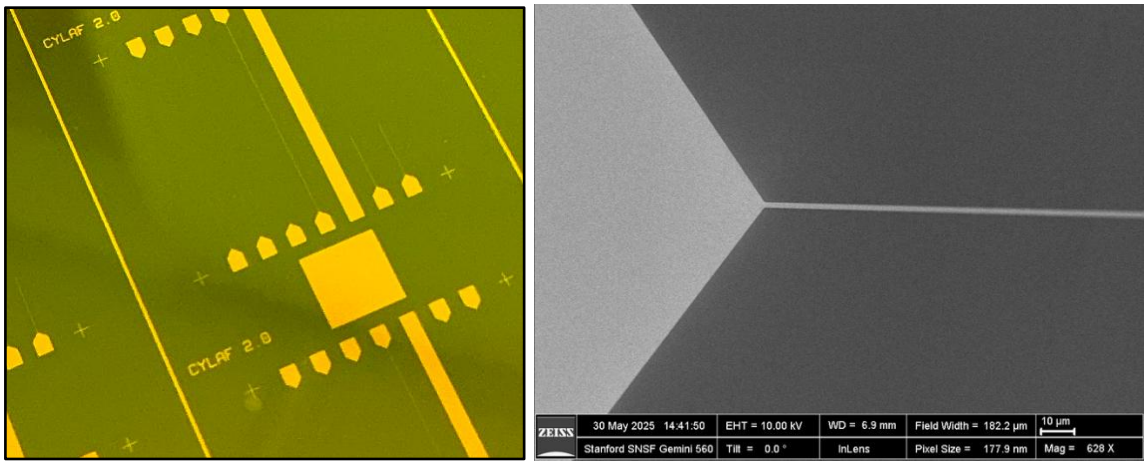

Fig. 8: Photograph (left) and SEM (right) of etched contacts and wires. W wiring (yellow/light grey) inspected to have no noticeable defects and clear contrast to underlying oxide (green/dark grey). SEM W wire width is measured to be 1.8µm.

	Our Values			*Hi-Quality*
W (μm)	*800*	*14.4*	*1.8*	-
t (nm)	20	20	20	20
L (mm)	12	12	12	-
R (kΩ)	2.8	140.4	1283	-
ρ (μΩ·cm)	**374**	**338**	**386**	**5.6**

Table 3: Comparison of measured tungsten resistivity across different metal shorts with expected resistivity from hi-quality thin-film tungsten

2.2.2. Silicon oxide coating

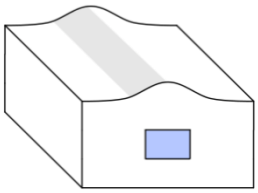

Fig. 9: SiO2 conformal deposition using CVD. Illustrated depiction.

While a PVD SiO_2 coating was attempted, using the Lesker2, micro-holes in the silicon oxide led to leakage in test devices. As a result, for this project we use CVD to deposit silicon oxide. The SiO_2 is deposited using CCP-DEP in the SNF, using the recipe *CCP-DEP SIO350-1* detailed more in Table 4. The SiO2 thickness is measured to be ~60-70nm on top of the tungsten, providing complete coverage to the wire sidewalls and protection in future etch steps for Ti + TiN.

Recipe	ccp-dep SIO350-1
Chamber Temp	350℃
Duration	60s
Thickness	~60-70 nm

Table 4: CVD SiO_2 Deposition Recipe. Details on chamber temperature, duration, and thickness used to deposit 70 nm of SiO_2

2.2.3. Via Etch

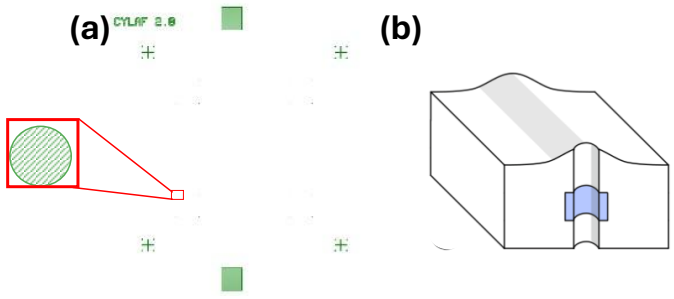

Fig. 10: Via etch "mask 2" with magnified view of the via (a) and 3D structure illustration (b). The mask also defines bottom / top squares to measure actual etch depth.

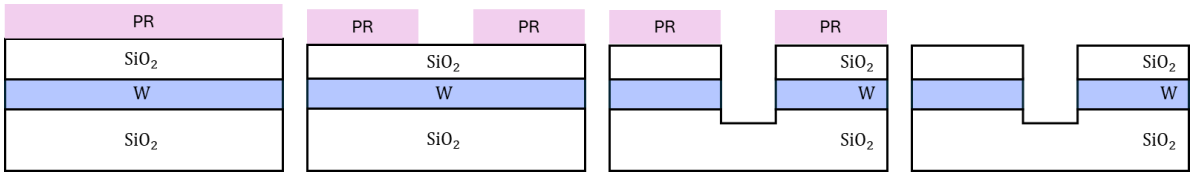

Fig. 11: Via Etch. Similar etch process to the wire etch, using a defined pattern in SPR3612 as a mask.

We use PT-MTL, recipe *W_SF6_N2_SWF1_bias*, similar to the one used for the initial tungsten wire patterning, to etch ~180 nm deep holes that punch through the SiO2 cap and the center of tungsten wires. We are reusing the characterization performed for the previous tungsten contact and wire etch step. Before and after stripping the photoresist, the pattern is optically inspected, shown in Fig. 12 and the depth of the etched via is measured via profilometer, through square test structures at the top and bottom of each chip.

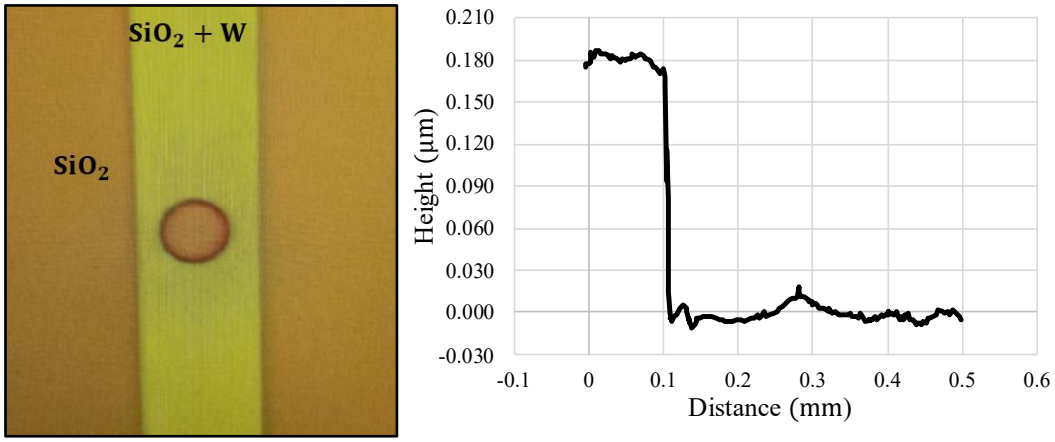

Fig. 12: Microscope (left) and profilometer (right) of etched vias. A small horizontal misalignment can be observed here on the largest 8 um via.

Gas concentration	SF6 30 sccm N2 30 sccm
Bias RF forward power	30 W
Pressure	5 mTorr
Main step duration	500 s
Etch depth	180 nm

Table 5: SiO2 + W dual etch recipe *W_SWF1_bias_ME_SF6_N2.* Details on gas concentration and power to etch W and SiO2 layer.

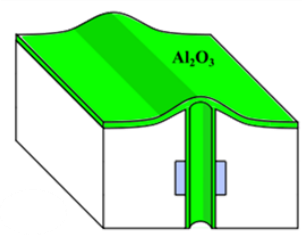

Fig. 13. ALD of aluminum oxide illustration.

Aluminum oxide is deposited using ALD on the Fiji2 in the SNF, modeled in fig. 13. Before depositing, a recipe characterization is run using the SNF *Standard Plasma Al2O3* recipe, as detailed in Table 6.

Precursor	TMAH $+ O_2$ Plasma
Chamber Temp	$200°C$
Å/Cycle	0.94
Cycles	100
Average Thickness (Å)	93.8
Nonuniformity (σ/μ)	4%

Table 6: ALD Al_2O_3 Recipe. Details on chamber temperature, duration, and thickness used to deposit 70 nm of SiO_2

As seen in Table 6, the ALD at the time of deposition had relatively low uniformity across the Fiji2 chuck depicted further in, shown in Fig. 14. Two potential sources of nonuniformity come from the chuck not being fully centered in the chamber, and multiple valves in the Fiji2 chamber being leaky during the deposition.

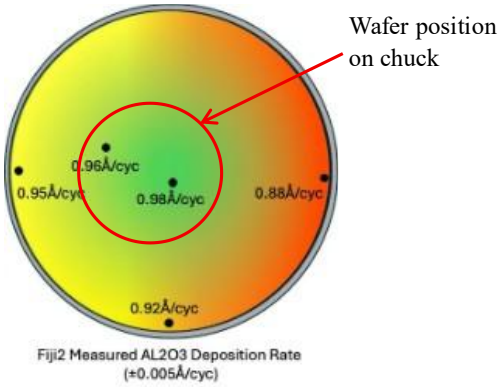

Fig. 14: Deposition nonuniformity across the Fiji2 chamber for Plasma Al_2O_3. Wafer positioning on chuck is illustrated for reference.

We deposit 53 cycles of Al_2O_3 using the same recipe, ensuring our wafer remains centered in the chuck, illustrated in Fig. 14. Measuring the alumina thickness following deposition to be ~5 nm.

2.2.4. Tungsten contact exposure

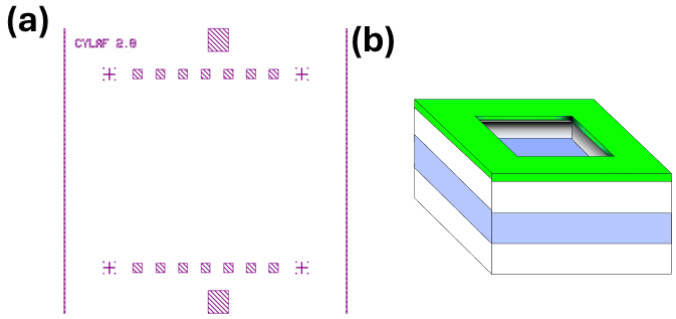

Fig. 15: Exposing tungsten contacts "mask 3" (a) and 3D structure (b).

To allow electrical connection with the tungsten contacts, the aluminum oxide and silicon oxide are selectively etched to expose the underlying tungsten (Fig. 15). This is done through a hard mask pattern, defined in the aluminum oxide, using the process flow described in A.2.2, followed by an HF-Vapor etch using the uetch in the SNF.

For our process, illustrated in Fig. 16, the Al_2O_3 is etched in MF26A for 7 minutes followed by a 30 second DI-water bath. We then strip the resist pattern using acetone for 2 minutes, and bake the wafer at 215 for 1 minute followed by an O_2 descum in the Samco for 1 minute. This removes all potential organics that could reduce selectivity of the vapor etch. We run uetch *Recipe 1* for 8 cycles, followed by two chamber purges to fully remove any remaining anhydrous HF.

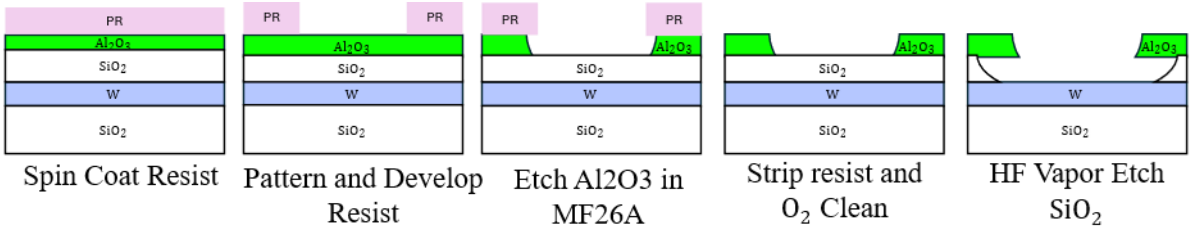

Fig. 16: HF-vapor etch process flow illustration

The resulting wafer is optically and electrically inspected to verify the tungsten contacts are exposed. Optically, tungsten is visibly contrasting against surrounding SiO_2 and Al_2O_3 (Fig. 17), and using a probe, we are able to measure continuity across the metal-short contacts.

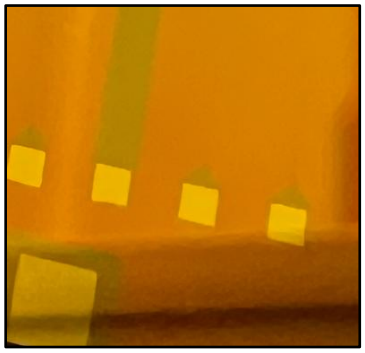

Fig. 17: Image of W contact exposure. Bare tungsten (yellow) contrasted with surrounding alumina and silicon oxide (orange/green).

2.2.5. Wafer partitioning for process split

To characterize the effect of different Al2O3 thicknesses (**5 nm, 7 nm, 9 nm**) on breakdown characteristics, and to test different deposition techniques for the TiN/Ti inner electrode, we proceeded with a wafer partitioning in 9 samples after the contact exposure. This was performed using the wafer saw (Fig.18) with the generous assistance of a classmate qualified on the tool.

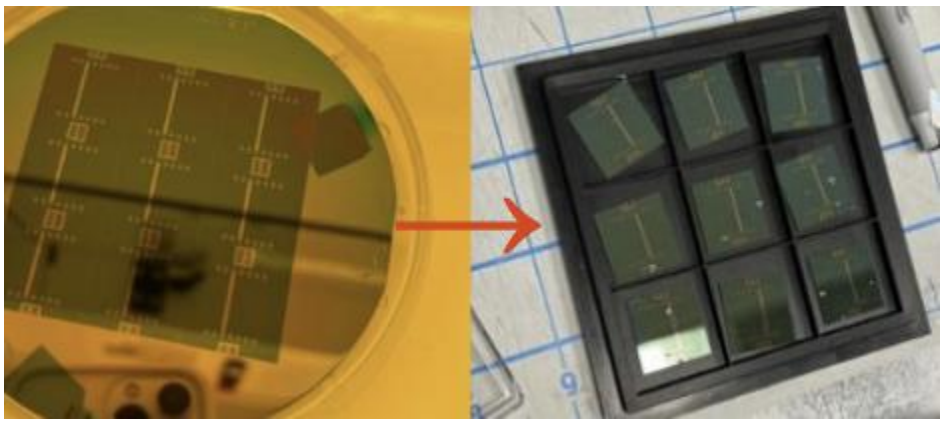

Fig. 18: Wafer partitioning into 3×3 chips. Each individual chip is now 2 cm × 2 cm.

2.2.6. Titanium nitride and titanium contacts and wires

Deposition of TiN and Ti PVD was done using the lesker2 sputter. Initial deposition rate characterizations were performed using long deposition durations (resp. 2000 s for TiN and 1440 s for Ti) and profilometer measurements using tape as mask. For TiN, RF sputtering was used, vs DC sputtering for Ti. Resistivity measurements were conducted on these thick films, and on the thinner final films, to estimate the voltage drop on the TiN/Ti wires.

Deposition	RF TiN	DC Ti
Power	100 W	200 W
Pressure	3 mTorr	3 mTorr
Duration	800 s	1080 s
Thickness	20 nm	108 nm
ρ (uΩ cm)	~67 000	~520

Table 7: PVD TiN and Ti Recipes. Details on power, pressure, and duration used to deposit 20 nm of TiN and 108 nm of Ti

Initially, a lift-off process was considered for this step to pattern the TiN/Ti wires, but it was abandoned because of the etching of the thin alumina layer by the developers. MF-26A etch was as expected > 1 nm / min, but we also characterized the wet etching of alumina Al2O3 by the AZ developer 1:1 at **0.4 nm / min** (initial alumina film thickness: 10.4 nm, 6 minute AZ bath, final alumina film thickness: 8.0 nm).

Consequently, the TiN and Ti layers were deposited unpatterned, and the inverse of the mask from Fig. 19 (a) was applied with heidelberg2 for etching.

Ti and TiN etching was made complex by the multi-layered metal structure to etch (Fig. 20). The objective of this etch step was to remove the Ti and TiN layers without attacking the underlying W base. The 5 nm Al2O3 and ~60-70 nm SiO2 layers served as barriers, allowing some overetching below the Ti layer.

After testing several Ti and TiN recipes, we used a modified *Ti_Mina* recipe using a high concentration of CL2 (assumed to be selective for Ti/TiN with slower attack on SiO2). We added a small concentration of BCL3 in an initial step to first remove the possible oxide layer on top of the Ti (Table 7,8). We tried different main step durations on multiple samples before settling down on 85 s for the main step to etch away the Ti/TiN layers entirely while avoiding W etching.

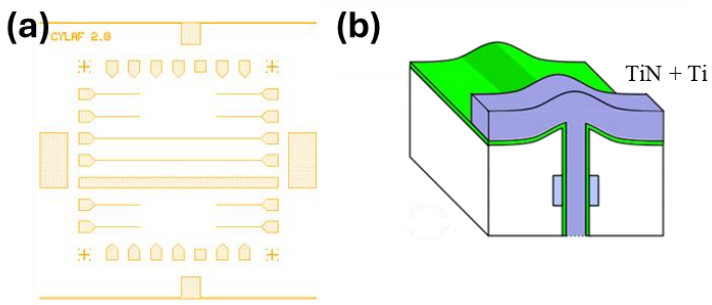

Figure 19: Defining TiN + Ti wire and contacts "mask 4" (a) with 3D structure (b).

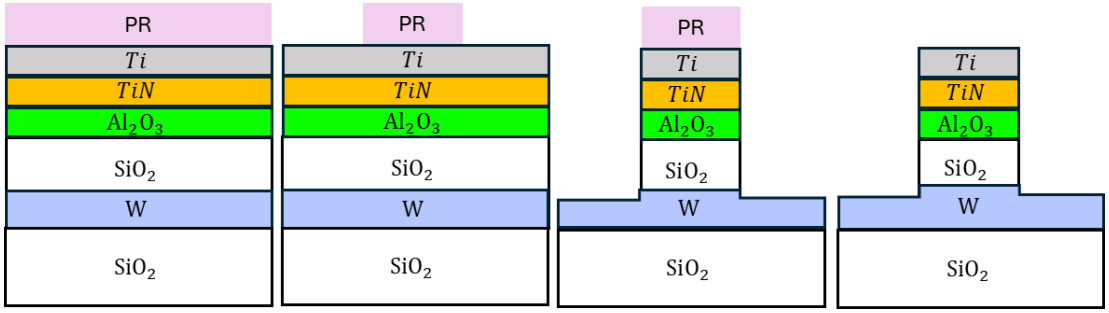

Figure 20: TiN + Ti wire and contact process flow. Wire and contact definition similar to previous wire etching, using a SPR3612 mask for feature definition and dry etch of sputtered metal.

First step concentration (no bias or ICP yet)	CL2 90 sccm BCL3 20 sccm AR 25 sccm
Main step concentration	CL2 95.2 sccm AR 5 sccm
Bias RF forward power	200 W
ICP RF Power	400 W
Pressure	10 mTorr
Main step duration	85s
Etch depth	~150-170 nm (est.)

Table 8: TiN + Ti dual etch recipe *Ti_Mina*

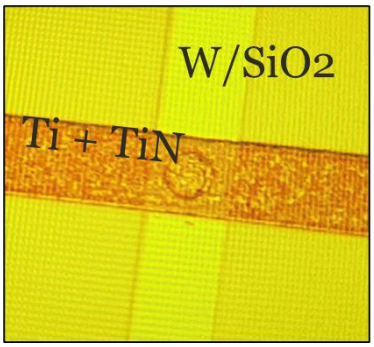

Figure 21: Final result of TiN + Ti wire and contact definition. TiN and Ti (orange) fill the defined via and the wire perpendicular to the tungsten wire.

	Our Values		*Hi-Quality*	
	Ti	*TiN*	*Ti* [8]	*TiN* [9]
W (mm)	*1.25*	*2*	-	-
t (nm)	144	50	35	35
L (mm)	80	30	-	
R (kΩ)	2.3	200	-	
ρ (μΩ·cm)	**520**	**67000**	**100**	**128**

Table 9: Ti an TiN Resistivity Measurements vs Hi-Quality Thin Films from literature search

2.3. Breakdown Measurement

The breakdown measurements are run on the Micromanipulator6000 in the SNF. To do so, we use two probes, placing them on the contacts corresponding to the desired antifuse, and run several I-V measurements to measure the pre-breakdown, breakdown, and post-breakdown resistance. All other contacts are left floating to prevent a current path through other antifuses.

Keeping the bottom (W) contact bias at 0V, we sweep voltage on the top (TiN) contact. The voltage sweep is summarized in Table 10, and described in greater detail below.

	V_{min} (V)	V_{max} (V)	V_{step} (V)
$Read$	-1	1	0.1
$Write$	-1	10	0.1

Table 10: Breakdown Measurement Conditions. Voltage sweep range and step size for read and write measurements.

Read Measurements: Pre-breakdown measurements and post-breakdown measurements are run from 0 to +1V then -1V in 100mV increments. A read voltage of 0.7V is selected for measuring on/off ratio.

Breakdown: We induce breakdown by sweeping voltage to +10V in 10mV increments, before sweeping back to -1V in 100mV increments. A read voltage of 0.7V is selected for measuring on/off ratio.

3. Results and Discussions

Due to misalignment issues and thinned Al_2O_3 from an initial think deposition and multiple etches in AZ1:1, we were limited in the number of testable antifuses. Despite this, using the test conditions described in 2.3, we were able to measure a significant change in resistance (Fig. 22 (b)) and current (Fig. 22(e)) during breakdown.

The cylindrical antifuse we tested broke down at an applied ~5.53V, achieving a 23.4× decrease in resistance from pre-breakdown (Fig. 22(a)) to post-breakdown (Fig. 22(c)) measurements. The measured breakdown occurs gradually from ~2.3-5.5V with an additional sudden breakdown occurring at 5.53V.

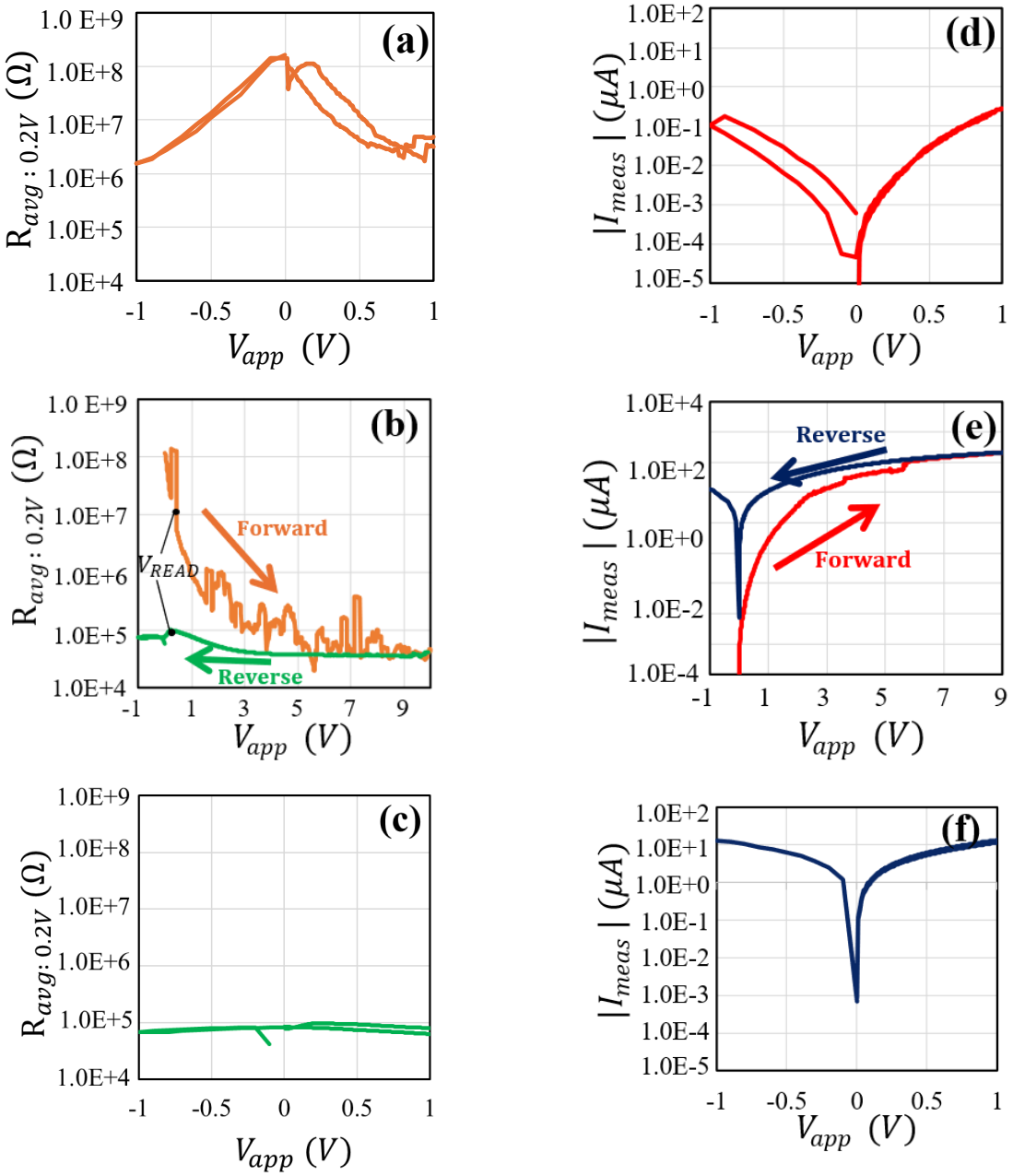

Fig. 22: Resistance (a-c) and current (d-f) measurements. Current and resistance are measured vs applied voltage before (a,d) during (b,e) and after (c,f) breakdown, showing a permanent change in resistance.

While a noticeable breakdown occurs, we see both relatively low pre-breakdown resistance (<5M Ω @ 0.7V) and higher than expected resistance after breakdown (>1 kΩ @0.7V), listed in Table 11. Based on our resistivity for both tungsten (Table 3) and TiN+Ti (Table 9), we expect to see a high resistance after breakdown. The resistance, dominated by the TiN via, is calculated to be approximately 80kΩ, matching the expected resistance in Table 11. From the thin Al_2O_3, we expect a breakdown voltage between 3.5 and 5.5 V (approximately proportional to the thickness

of the oxide). The thin, potentially non-uniform aluminum oxide also presents as a source for current leakage.

D_{hole}	8 µm
V_{BR}	5.53 V
R_{hi} @ 0.7V	2.34×10^3 kΩ
R_{lo} @ 0.7V	87.3 kΩ
R_{hi}: R_{lo} @ 0.7V	26.8×

Table 11: Measured cylindrical antifuse breakdown characteristics. Resistance before and after breakdown show a 26.8 × decrease in resistance after breakdown.

Given the high resistance of the deposited TiN and high chamber pressure of the Lesker2, it is proposed that the deposited metal is closer to $Ti_xN_yO_z$, as the TiN most likely oxidized. Additional XPS measurements would be needed to verify, but the chemistry matches the gradual breakdown of Ti + Al_2O_3 MIM stacks, allowing for a more accurate comparison, we compare our normalized breakdown curve to the breakdown curves of various Al_2O_3 thicknesses published by M. Tian et al. [10], shown in Fig. 23

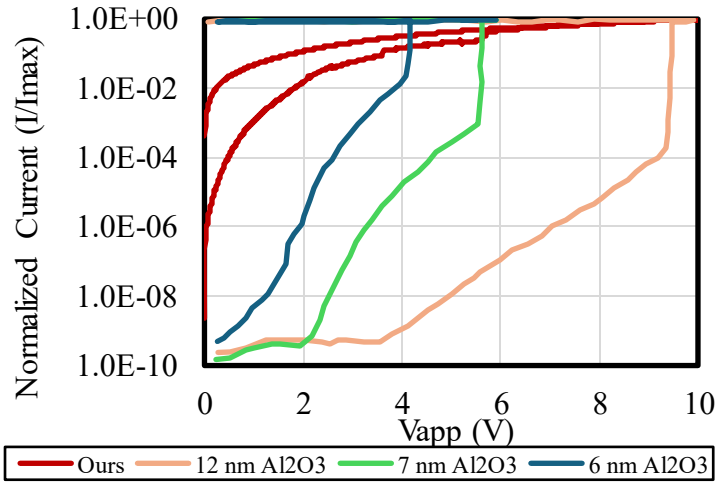

Fig. 23: Comparison of different Al_2O_3 thicknesses in a planar Ti + Al_2O_3 MIM Stack [10] **with our $Ti_xN_yO_z$ + Al_2O_3 MIM stack.** Comparison of normalized currents versus breakdown voltage. Breakdown sharpness and voltage scale proportionally with alumina thickness.

4. Future Work

After E241, we plan to expand on this project along the following paths:

Improving Oxide Barrier: We aim to improve the Al_2O_3 by rerunning the process with a better ALD uniformity and characterizing the oxide across multiple thicknesses to achieve better breakdown. We will optimize the ALD recipe to decrease the pre-breakdown oxide leakage and

improve the capacitance. We also plan to measure multiple thicknesses of Al2O3, which was initially planned for this course, but had to be dropped due to time constraints. Using several process splits, we can characterize a reliable high-performance oxide for future antifuse tests.

Smaller Feature Sizes: We plan to rerun this process using e-beam lithography to compare planar and cylindrical antifuse performance at extremely scaled nodes. From this comparison, we plan to compare performance scaling with decreasing feature size between planar and cylindrical antifuses as well as inform future simulations for scaled process nodes.

BiCS Fabrication Process in SNF: The main benefit of the cylindrical antifuse is the bit-cost scalable process flow. After demonstrating the proof of concept for the antifuse, our next step is to rework our fabrication process, so complexity becomes layer-independent. This will allow for future work in multi-layer designs, and present additional opportunities for a self-aligned scalable process. Additional BiCS work will then be done on non-breakdown-based devices. We plan to fabricate pre-connected wires using just a top-mask and stair-stepped resist structures.

Conclusions

In our project we designed, fabricated, and tested cylindrical antifuses. Through optical lithography, we designed MIM antifuses using tungsten, aluminum oxide, and titanium nitride. We then measured the breakdown conditions of the fabricated antifuses. We found that high resistance metal deposition and a thin oxide breakdown layer degraded the quality of the antifuse, leading to a high leakage current of ~300nA pre-breakdown, and relatively low on current of ~8μA post-breakdown. Despite this, we were able to successfully able to demonstrate a one-time change in resistance through controlled breakdown through the aluminum oxide layer. This proof of concept generates potential future work improving the antifuse electrical performance and expanding the process to one with layer-independent complexity.

Acknowledgement

We would like to thank our mentors for all of their help and support on this project, without whom this would not have been possible. Thank you, Swaroop Kommera, for being our faculty mentor, and your help and guidance in developing our process flow and connecting us with the SNF staff. Thank you, Don Gardner, for being our industry mentor, and your deeper insight into specific fabrication and characterization processes. We would also like to thank peers and mentors outside of the course for their assistance with process flow design. We are grateful to Shengman Li defining our photolithography process, Hugo Chen for his advice in etching, deposition, and liftoff, and Nate Saffron for refining the HF-Vapor process. Thank you to the SNF staff for your help and support in training and advising us on different steps throughout the process. Thank you, Lavendra, Grant, Uli, and Sarah, for your training and advice, Alex for your support and feedback, and Carson for helping us with setbacks and mistakes. Finally, we are especially grateful for the entirety of the E241 team, groups, and mentors for this experience. Thank you, Debbie Senesky,

for organizing the course and allowing us to pursue this project, other team's mentors, for your feedback and comments on our weekly presentations, Sergio for helping this class move smoothly, and other teams for your consistently useful advice on how to improve our process flow.

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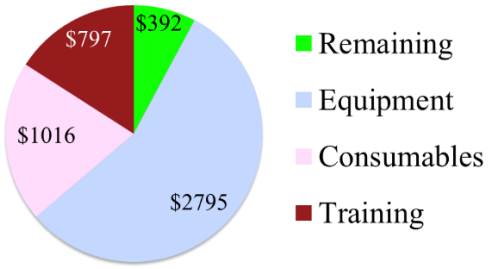
Appendix

A.1. Budget

This class served as an introduction to the SNF, requiring training across several tools and basic equipment for processing. However, over half of the budget was spent across several tools, including the Lesker2, Fiji2, PT-MTL, and Heidleberg2.

Total Budget: $5,000



A.2. Standard Operating Procedures

A.2.1. Shipley 3612 Optical Lithography

Step	*Tool*	*Instructions*
Prime	YES Oven	Clean the wafer using IPA and N_2 dry, then run Recipe 1 for a singe and HMDS prime to promote resist adhesion
Resist coat	Headway2	Coat 3612 at 5500 RPM for 40 seconds.
Bake 1	Hotplate	Bake resist at 90°C for 1 minute.
Exposure	Heidelberg2	Expose the gate pattern and alignment marks on Heidelberg with dose 80 mJ/cm^2
Bake 2	Hotplate	Bake at 1 115°C for 1 min
Develop	Developer Bench	Develop for 60 seconds in MF26A, rise with DI water 30s and blow dry. Check developed pattern using an optical microscope.
Strip	Solvent Bench	Soak in Acetone at room temperature with pipette agitation. Rinse with acetone followed by IPA. N_2 Dry so no spots occur
Check	Microscope	Inspect in optical microscope that no resist or residue remains.

To ensure a clean resist spin, be sure to fully clean and dry the wafer or piece before spinning. If you are manually spinning resist via pipette, use a new, clean pipette. Squeeze the

pipette to push out the air and lower the pipette halfway into the resist to prevent dried resist contamination. Then deposit the resist onto the center of your piece and immediately begin spinning. Once the spinner is finished, check the resist for streaks, and remove any backside resist with a cleanroom swab.

A.2.2. HF-Vapor Etch Hardmask

Step	***Tool***	***Instructions***
Deposit Al_2O_3	Fiji2	Run the *Standard Plasma Al_2O_3* recipe for 50 cycles for 5nm Al_2O_3. Include a dummy wafer with measured oxide thickness
Measure Thickness	Woollam	Measure the thickness of the deposited Al_2O_3 on the dummy wafer
Define Mask	Heidelberg2	Define and develop your desired mask pattern. Process defined in A.2.1 for using SPR 3612 photoresist. *A mask smaller than your desired exposed area (by 3-5 nm on all sides) is recommended to allow over etching in the next step*
Develop	Developer Bench	Etch in MF26A 1 minute per nm of Al_2O_3, rise with DI water 30s and blow dry. Over-etch if possible to ensure exposed oxide
Strip	Solvent Bench	Soak in Acetone at room temperature with pipette agitation. Rinse with acetone followed by IPA. N_2 Dry so no spots occur
Check	Microscope	Inspect in optical microscope that no resist or residue remains.
Clean	Samco	Run an O_2 descum for 1 minute with the wafer on the bottom shelf