Optimized Electron Beam Resist Reflow for High-Q Photonic Resonators

ENGR 241 Spring 2025 Final Report

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1 Introduction

1.1 Photonic Resonators

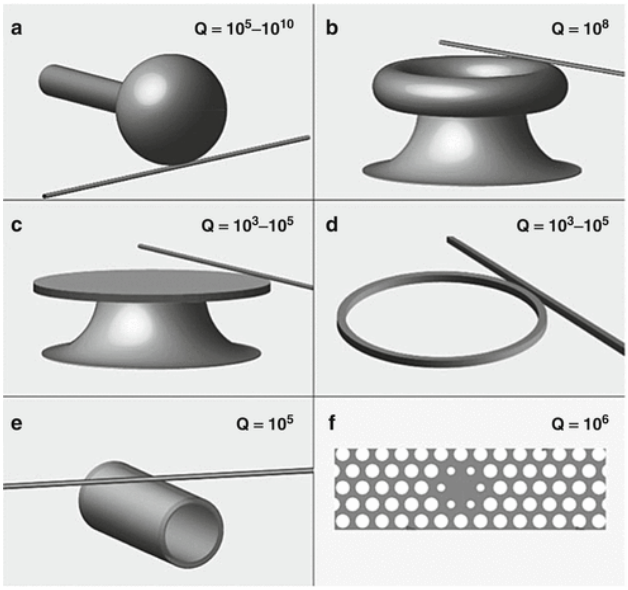


Figure 1: Various photonic resonator geometries commonly encountered in integrated photonics for trapping light. **(a)** Spherical resonator. **(b)** Toroid resonator. **(c)** Disk resonator. **(d)** Ring resonator. **(e)** Cylindrical resonator. **(f)** Photonic crystal cavity. Figure reproduced from Ref. [1].

Photonic micro- and nano-resonators are devices made from optically transparent materials that trap optical fields for an extended period of time before the field exits or decays into the environment, while providing a small footprint and strong field intensity that are much harder to achieve in free-space mirror-based cavities. Such resonators can have various geometries, such as spheres, rings, disks, and photonic crystals (Fig. 1). Because of sharp resonance peaks and high sensitivity to the outside environment, such devices have applications in communications, signal processing, and biosensing. The combination of high confinement and long lifetime also allows for enhancement of optical nonlinearity, such as four-wave mixing and optical parametric processes, as well as an efficient interface for single-atom-single-photon interaction that finds application in quantum networking and quantum computing.

A common figure of merit to quantify the performance of a photonic resonator is its quality factor Q. The quality factor characterizes how long a photon is trapped in the resonator before it gets absorbed or escapes the resonator due to out-coupling or scattering. Specifically, it is defined as

$$Q = 2\pi \frac{\text{stored energy}}{\text{energy lost per cycle}}$$

or equivalently $Q = \omega/\kappa$ where ω is the resonant frequency and κ the loss rate.

For various applications in nonlinear and quantum optics, an appropriate figure of merit is Q/V, the ratio of quality factor Q over optical mode volume V. Mode volume describes how strongly the mode is confined. Stronger confinement can improve nonlinear optical processes since they are dependent on $V^{-\alpha}$ for α a positive real number. For example, optical parametric process threshold scales as Q^2/V, and single-photon-single-atom interaction infidelity scales with $\sim V/Q$. Therefore, improving Q and decreasing V have been viewed as the primary ways to improve the performance of photonic resonators.

1.2 What Limits Optical Quality Factor?

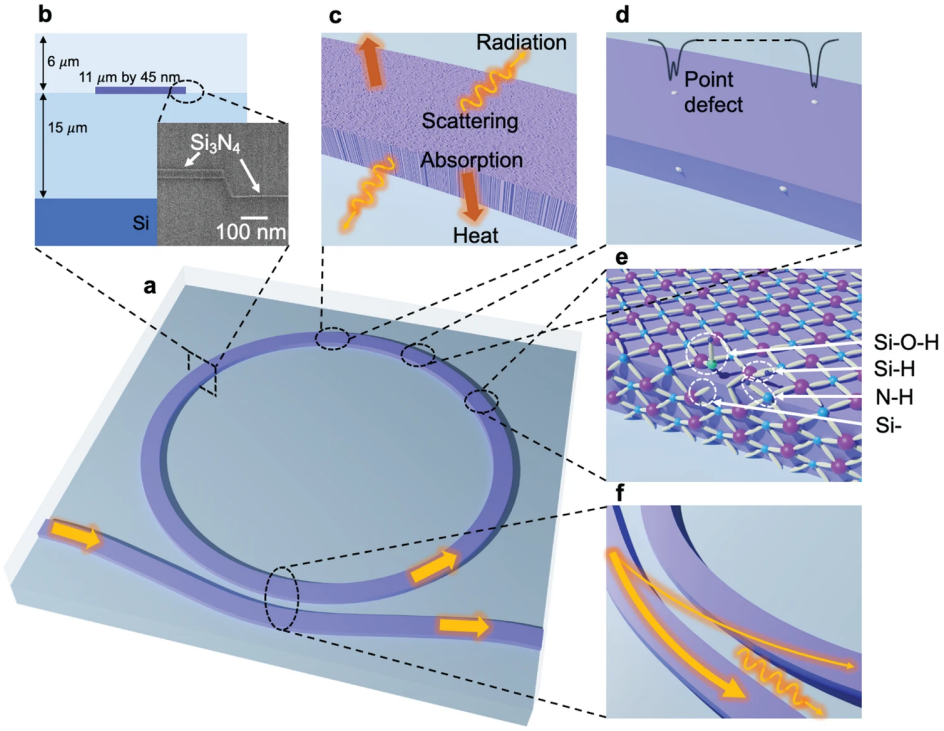


Figure 2: Various loss mechanisms in an integrated photonic platform coming from the material itself and imperfect geometries on the device. Figure reproduced from Ref. [2].

Integrated photonic devices have various loss mechanisms that limit the ultimately achievable quality factor. We classify these mechanisms into material-intrinsic and material-extrinsic types.

Material-intrinsic: These loss mechanisms are found within the material itself and are typically related to optical bandgap, formation of surface states, crystalline defects, and phonon-assisted processes. A wide-bandgap material provides a large region that forbids the material's electronic states from forming, thereby preventing optical photons from being absorbed by such states or phonon-assisted processes. However, most (crystalline) materials are not perfect and will inevitably have the formation of mid-gap states from the surface that increase unwanted absorption losses. Crystalline defects such as grain boundaries, dislocations, and interstitial defects can also introduce scattering channels that will hamper

optical field propagation. Most of these optical absorption and scattering processes can be mitigated by improving the crystal or material quality and thereby providing a nearly ideal material to work with.

Material-extrinsic: Since many crystalline and amorphous materials used in integrated photonics are generally of very high quality, intrinsic material absorption losses are, to some extent, less of a problem. In practice, factors extrinsic to the material itself are the dominant loss mechanisms for photonic resonators, and these generally include surface and sidewall scattering. Surface roughness due to imperfect thin-film processing or introduced via poor etch chemistry/resist quality generates scattering processes on the surface of an optical mode, while sidewall roughness from etching/resist roughness can contribute significantly to loss, even at Q-factors around 10^6. Since Q scales with $1/\sigma^2$ for sidewall and surface roughness, where σ is the root-mean-square value of roughness, reducing roughness in fabricating photonic resonators provides ample room for improving Q.

1.3 Photoresist Reflow

A key factor in improving the quality factor of photonic resonators is reducing the surface and sidewall roughness. For surface roughness, thin films deposited by chemical vapor deposition (CVD) or made by the grind-and-polish method already achieve sub-nanometer roughness, and are perhaps mainly limited by etch chemistry. For sidewall roughness, the roughness can be introduced from an imperfect resist-substrate interface, resist roughness, or nonuniform etch.

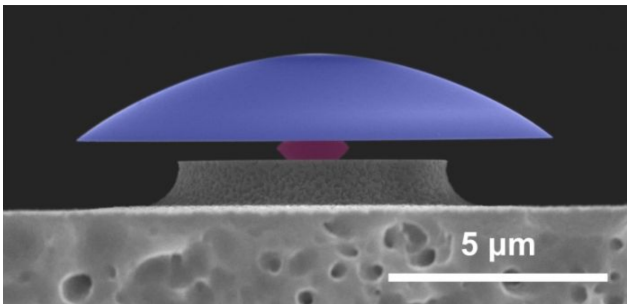


Figure 3: A mushroom-shaped 4H-SiC disk resonator. The smooth profile is achieved using photoresist reflow. Figure reproduced from Ref. [3].

One method to improve resist roughness and resist-substrate interface imperfections is thermal reflow. In this process, developed resist is heated above the glass transition temperature to create an atomically smooth surface. This method is especially common in photolithography and has been used to achieve 0.3 nm surface roughness in 4H-SiC resonators [3], resulting in a quality factor exceeding 10^6 at 916 nm wavelength (Fig. 3).

1.4 Electron Beam Resist Reflow

While photoresist reflow is well established for fabricating smooth disk resonators, photolithography cannot be used to fabricate small features with high resolution due to the

diffraction limit of light. Small features could include ring resonators and photonic crystals with nm and µm-scale feature sizes, where electron-beam (e-beam) lithography is commonly used to pattern high-resolution devices.

Therefore, in our project, we focus on developing a process for e-beam resist reflow. Although there is less literature about using e-beam resists for reflow processes, there are results of successfully improving sidewall roughness with thermal reflow of ZEP520A (Fig. 4).

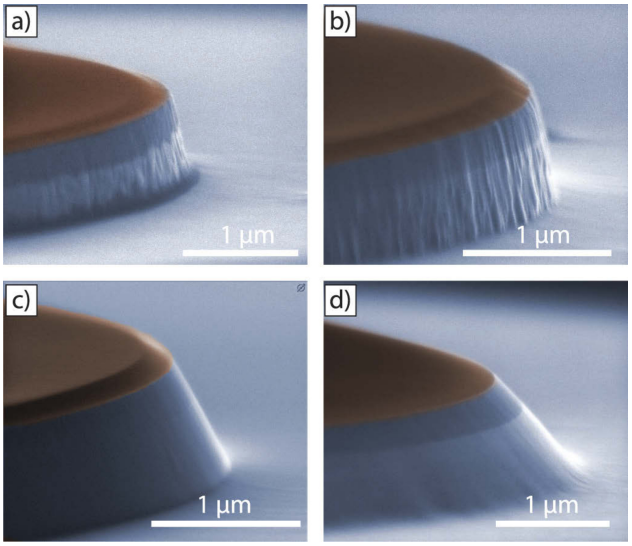


Figure 4: Electron beam resist reflow for fabrication of GaAs disk resonator, with the resist (ZEP520A) false-colored as red. (a) No reflow, (b) 140 °C reflow for 2 minutes, (c) 160 °C reflow for 2 minutes, (b) 180 °C reflow for 2 minutes. Notice the sidewall roughness generally improves with higher temperature, although there is an optimal temperature for successful reflow. Figure reproduced from Ref. [4].

ZEP520A is a high-resolution positive electron beam resist that is widely used in electron beam lithography. A related resist is CSAR62, which has similar chemical properties. Being a positive resist, ZEP520A does not cross-link upon exposure like negative resists – such as HSQ – do, and thereby allows thermal reflow to occur. For ZEP520A, its glass transition temperature is reported to be between 105 °C and 145 °C [5], making the resist suitable for thermal reflow by using a cleanroom hotplate. We note that the reflow dynamics of ZEP520A are dependent on several factors: the age of resist, exposure dose, reflow time, and temperature.

In our reflow experiments, we aim to study reflow temperature, as from the literature, this has the strongest impact on the device quality. We want to minimize surface and sidewall roughness while preserving structural integrity, such as coupler distance, waveguide width, and preventing collapsing features. While higher temperatures or longer reflow times tend to produce smoother surfaces, they can induce collapsing features and slanted sidewalls. A sweet spot can be achieved by finding an optimal reflow temperature slightly above the glass transition temperature that reduces sidewall roughness without significantly affecting feature geometry.

2 Project Overview

2.1 Project Goals

The goal of this work is to realize a method for reflowing ZEP520A, a common e-beam resist used in SNSF, to fabricate high-Q resonators while overcoming the diffraction limit of photoresist reflow using near-UV or violet optical lithography in SNF. Such fabrication process can yield devices with feature sizes smaller than 300 nm, which is required for single-mode near-infrared guiding in waveguides. In addition, we are also interested in ZEP520A reflow dynamics, as the reflow recipe for photoresist to fabricate SiC resonators so far fails to preserve coupling regions between waveguides and resonators (see Fig. 5).

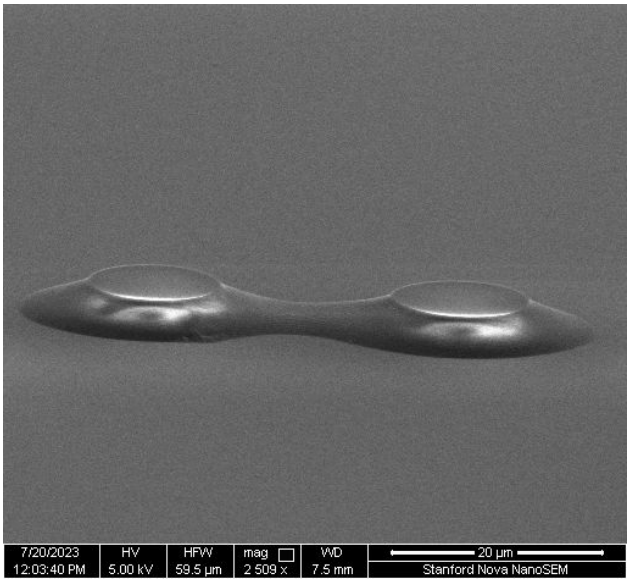


Figure 5: SEM of photoresist reflow for a coupled-resonator device on silicon carbide. Notice that the reflowed photoresist structures tend to clump together, making photoresist reflow incompatible with more complex device fabrication.

Thus, the deliverables of our project are

- **Develop an understanding of reflow dynamics of e-beam resists, focusing on ZEP520A:** The goal is to determine the optimal parameters (temperature, feature size, exposure dose) to make e-beam resist reflow successful for resonator fabrication.
- **Develop a high-yield e-beam reflow process that reduces surface and side-wall roughness for micro- and nano-structures in Si/SiN:** This goal will be combined with etch processes to fabricate test structures for calibrating and optimizing reflow.
- **Fabrication of high-Q optical microresonators in Si/SiN:** This goal will inform us of the improvement on quality factor that e-beam reflow can bring for photonic devices.

2.2 Benefits to SNF/SNSF

Electron beam lithography remains the workhorse of many advanced fabrication projects in the Stanford research community, especially in integrated photonics, electronics, and quantum science. Furthermore, an understanding of how to use e-beam resist for fabricating ultra-high-quality micro- and nano-structures is of great importance for not only our research effort, but also for the wider Stanford Nano community in SNF (Stanford Nanofabrication Facility) and SNSF (Stanford Nano Shared Facilities). Therefore, our projects aim to achieve the following impact:

- **E-beam reflow recipe:** To our knowledge, e-beam resist reflow has not been thoroughly characterized or used for device fabrication at Stanford. Systematic study helps us determine the ability to develop an optimal ZEP520A reflow recipe that the nano@stanford community can use.
- **Widespread applications:** Improved e-beam resist reflow enables smaller structures with lower roughness, and does not have to be restricted to nanophotonics. For example, optomechanics and superconducting circuits heavily use e-beam for fabrication.
- **Material-agnostic:** E-beam resist reflow recipes can be straightforwardly applied to various materials such as Si, SiN, SiC, Sapphire, GaAs, GaN, and diamond, which are used by many research groups using SNF/SNSF facilities.

3 Process Development

In our project, we used the following process flow (Fig. 6) to fabricate silicon nitride (SiN) photonic devices with ZEP520A reflow.

3.1 Process Overview

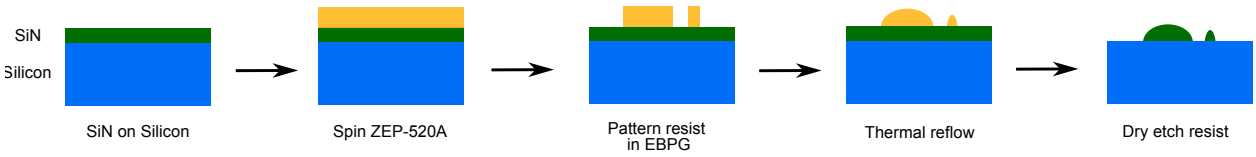


Figure 6: Process flow for fabricating resonator and waveguide structures on silicon nitride.

In detail, the process steps are

1. Deposit 290 nm thick LPCVD silicon nitride film on silicon wafer (Tystar, completed before this project)
2. Spin coat ZEP520A (SNSF, Section 4.1)
3. Pattern using e-beam lithography, develop, and cleave into smaller samples (EBPG5200+, Sections 4.2 and 4.3)
4. Thermal reflow of ZEP520A (SNSF, Section 5)
5. Dry etch SiN and strip remaining ZEP520A (Ox-RIE, Section 6)
6. Characterize reflowed ZEP520A and etched SiN devices (Park NX-10 AFM, Zeiss Gemini SEM, Sections 7 and 8)

3.2 Test Devices

To study reflow dynamics on common photonic structures, we make a `.gds` file with test waveguides and resonators. We sweep waveguide widths from 200 nm to 3000 nm and resonator radii from 10 µm to 50 µm. For ring resonators, we add another waveguide to test waveguide coupler structures during reflow. The resonator waveguides have a width of 1.2 µm and a coupler gap of 400 nm, common values for silicon nitride single-mode waveguides. These standard photonic test structures will provide information on the compatibility of ZEP520A reflow with more complex photonic integrations that require coupling light in/out.

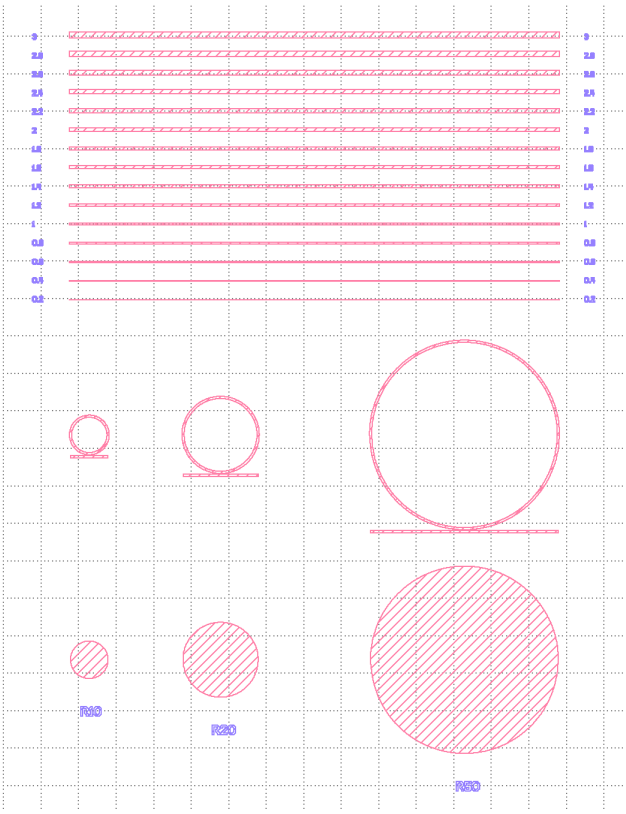


Figure 7: GDS file with photonic structures and devices for testing e-beam resist reflow. **Top:** Waveguides, **Middle:** Ring-resonators with out-coupling waveguides, **Bottom:** Disk resonators.

4 Device E-beam Lithography

4.1 Spin-coating ZEP520A

In the first step of our process, we cleaved a SiN/Si wafer into a $\sim$35 $\times$ 35 mm piece to fabricate a 6×6 matrix of test samples. We then spin-coated ZEP520A, using the following recipe:

1. Pre-bake sample at 180 °C for 3 minutes, then cool down for 1 minute
2. Spin ZEP520A at 5000 RPM for 1 minute
3. Post-bake substrate at 180 °C for 3 minutes, then cool down for 1 minute

Our first spin-coating failed as the resist was contaminated (Fig. 8). Therefore, we stripped the resist with Remover PG (3 min) and isopropanol spray. For the second try, we used a newer ZEP520A bottle, and the resulting layer was clean.

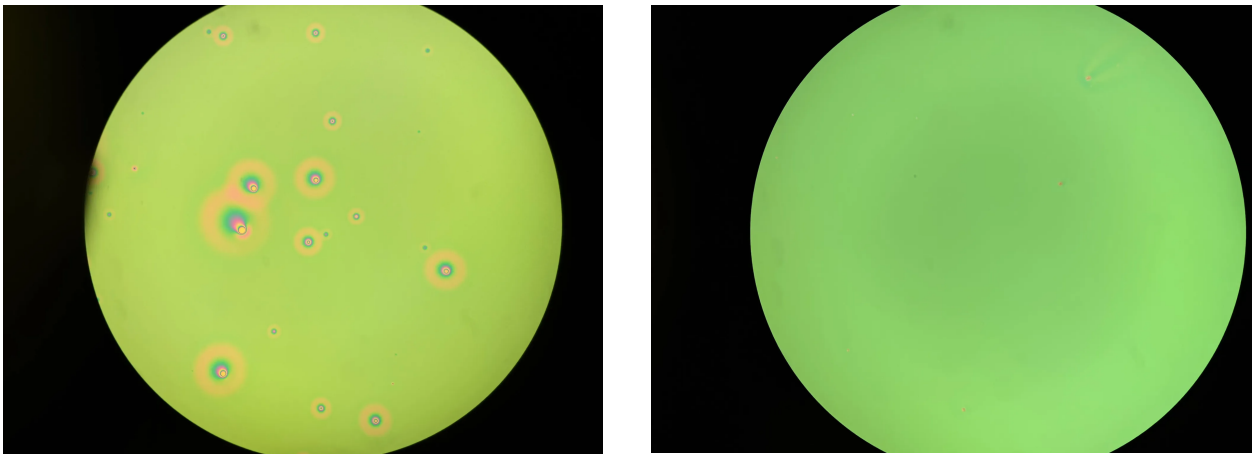


Figure 8: Spin-coated ZEP520A layer through an optical microscope. The first spin-coating was dirty (left), while the second one was clean (right).

4.2 Patterning

Pattern preparation: For a positive resist like ZEP520A, the exposed resist will be removed upon developing. To write devices on positive resist, we define 10 µm wide trenches around the device region in the `gds` file, leaving the resist on the to-be devices unexposed. Upon developing, the exposed resist will be removed, leaving open a pattern for transfer during etching.

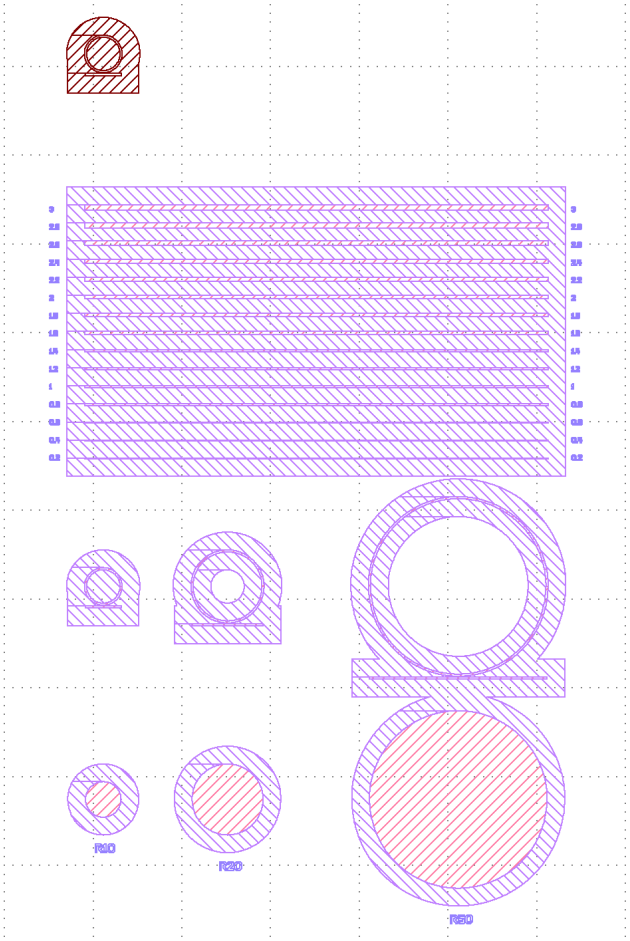


Figure 9: Pattern GDS file, where the shaded purple and brown regions define the exposed area.

EBPG write parameters: In practice, lithography is not a process that perfectly exposes resist for a given pattern and leaves the rest unexposed, nor does it have infinite resolution. With these practical limitations in mind, we need to carefully pick beam current, step size, aperture, dose, and proximity error correction, so that a write can be as accurate as we would like to. For our pattern and material stack, we opted for the following write parameters

- Step size: 10 nm
- Current: 5 nA
- Main device dose array: double pass 100, 125, 150 µC/cm^2 (i.e., total 200, 250, 300 µC/cm^2)
- 10 µm ring dose array: double pass 75, 87, 99, 111, 123, 135, 147, 159, 171, 183, 195 µC/cm^2 (i.e., total 150, 174, 198, 222, 246, 270, 294, 318, 342, 366, 390 µC/cm^2)
- Proximity error correction: SiN on SiO_2 on Si
- Field order: floating

- Feature order: follow geometry

Exposure and develop: We patterned the devices on EBPG2. With 36 devices in total and three doses per set, the total writing time was 1 hour and 5 minutes. We then developed the devices:

1. Develop in Xylene for 40 seconds
2. Soak in MIBK:IPA 1:1 for 30 seconds
3. Soak in IPA for 30 seconds

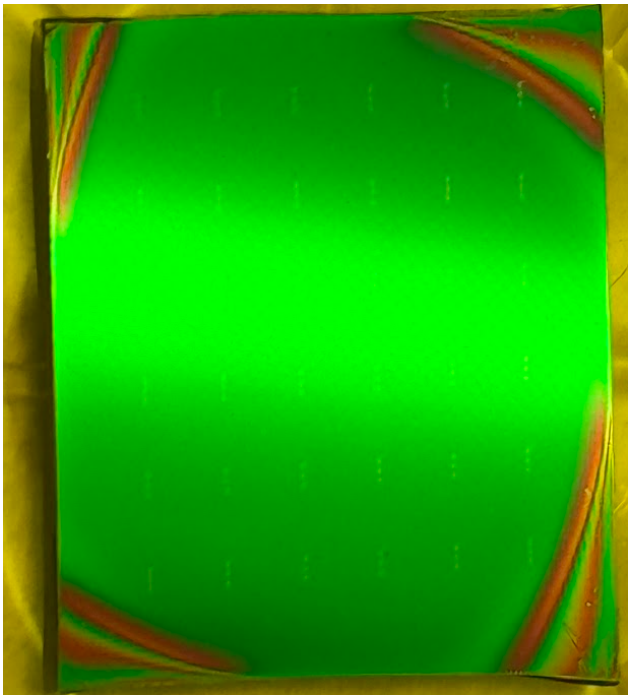


Figure 10: Post-developed SiN chip. The lighter colors dots arranged in a regular grid are the patterned devices, and the colorful fringes at the corners are from non-uniform ZEP520A spinning.

We verified that all devices survived development, demonstrating the high yield of the development process. An example device is shown in Fig. 11.

Devices with 150 and 176 µC/cm^2 total dose were underdeveloped, while devices with higher doses developed well. For the main structures, devices with 200 µC/cm^2 total dose were sometimes underdeveloped (purple color), while devices with 300 µC/cm^2 were sometimes overdeveloped (parts of the narrowest waveguide disappeared). Therefore, for the following experiments, we mainly focused on the devices with a medium total dose (250 µC/cm^2).

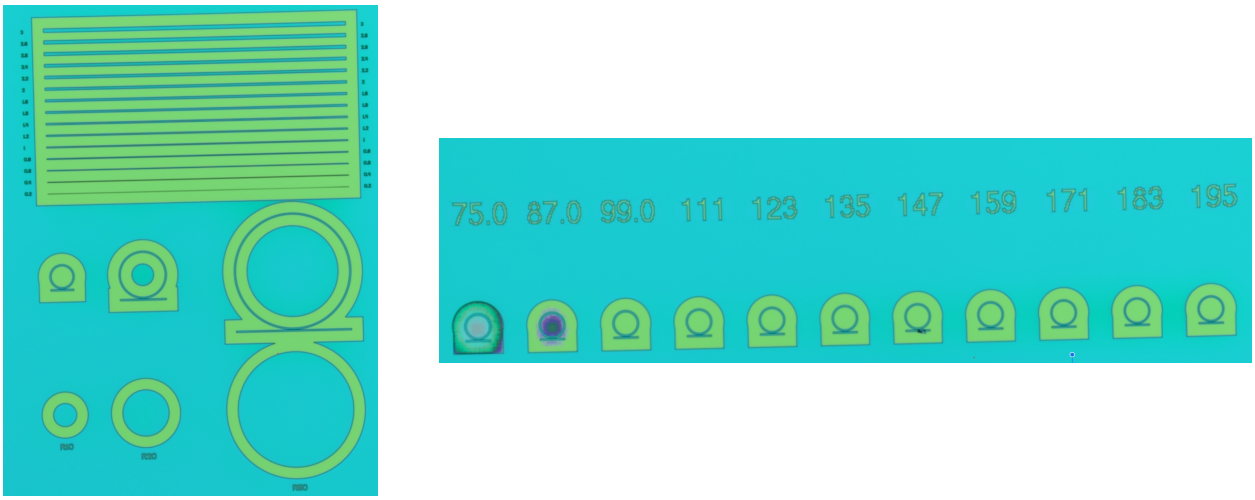


Figure 11: An example post-developed device before reflow (left) and dose array (right). ZEP520A is blue, while the yellow trenches are regions with ZEP520A removed (exposed SiN). The numbers indicate the dose ($\mu C/cm^2$) for one pass in a double pass development, so the total exposure dose is twice as high.

4.3 Device cleaving

To sweep various reflow parameters, we cleaved our chip into 36 smaller samples (each approximately 5×5 mm). The cleaving was conducted by making a mark with a diamond scribe, aligning the chip on a glass slide, and carefully applying pressure on the sides of the chip (see Fig. 12).

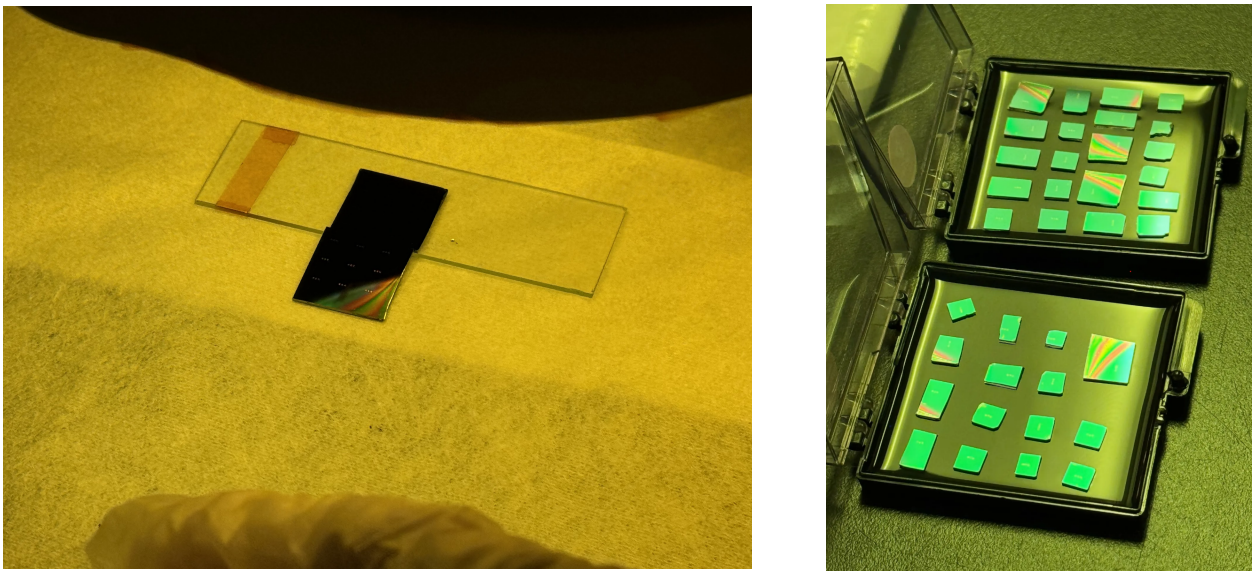


Figure 12: Cleaved SiN chips using a glass piece and applying pressure via tweezers.

5 ZEP520A Reflow Experiments

5.1 First Test

To roughly estimate the temperature range where ZEP520A reflows and to practice the reflow process, we first performed a test run on one ZEP520A sample with increasing temperatures. The reflow time was fixed at 2 minutes as suggested by the literature, followed by a 1-minute cool-down on the metal surface of the wet bench. For the first test, we used the custom-made triple hotplate in SNSF (Fig. 13). The results are listed in Table 1, and illustrative microscope images are shown in Figures 14 and 15.

The reflow time was chosen to be short, as a long reflow time will inevitably collapse the microstructures (see Ref. [5]), thus rendering the reflow impractical for pattern transfer. In the literature, we found that a reflow time of less than 5 minutes can preserve microstructures while inducing resist self-healing.

Figure 13: SNSF triple hotplate. Due to suboptimal feedback control, the temperature setting (green) can vary significantly from the temperature reading (red).

Temp. (setting)	**Temp. (reading)**	**Measured temp. (IR)**	**Observation (optical microscope)**
105 °C		112–114 °C	No reflow observed, resist did not melt.
115 °C	123 °C	129 °C	Edge starts to melt very slightly, can see a slightly different focus on the edge versus the top surface.
129 °C		138–142 °C	Prominent reddish boundary for rings and disks. No evidence of reflow for other devices.
140 °C	146 °C	152–153 °C	More prominent reddish boundary for rings and disks. No evidence of reflow for other devices.
150 °C	156 °C	164 °C	More prominent reddish boundary for rings, waveguides, and disks as seen from thin-film interference.

Table 1: First reflow test temperature settings and observations

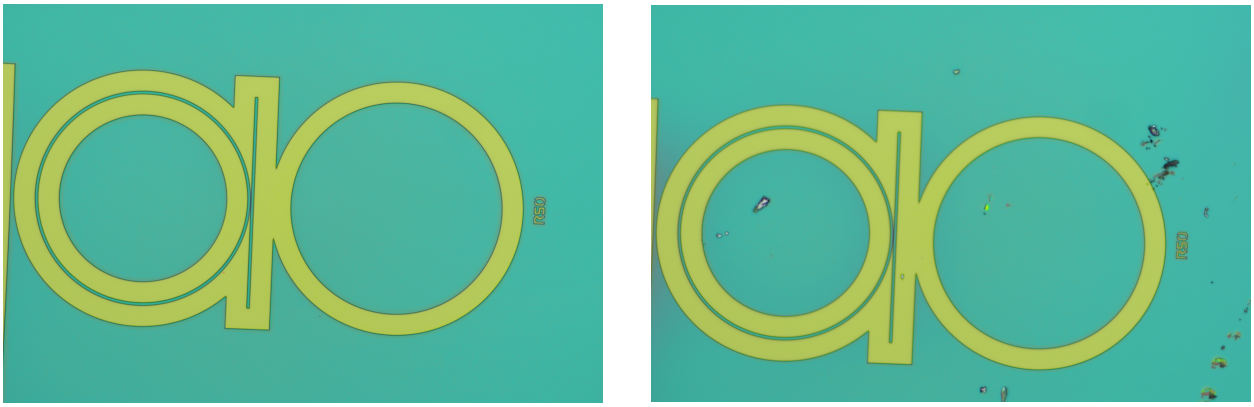


Figure 14: First reflow test sample after heating at 140 °C, lowest dose (left) and highest dose (right).

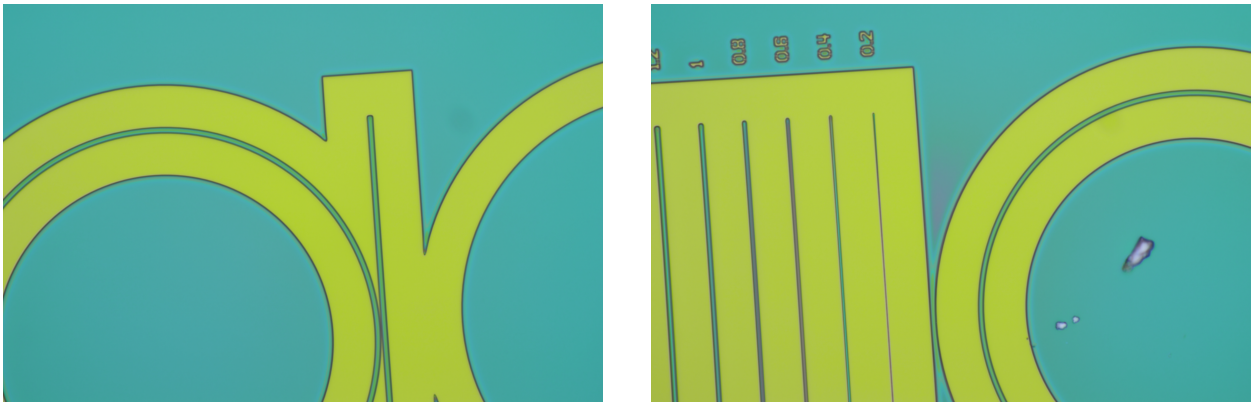


Figure 15: First reflow test sample after heating at 160 °C, lowest dose (left) and highest dose (right).

We noticed that the triple hotplate struggled to stabilize temperature, with the temperature reading significantly deviating from the setting. In addition, an infrared (IR) thermometer consistently measured 5–10 °C higher temperature than the hotplate reading. Therefore, we decided to run a second test with a different hotplate in SNSF.

5.2 Second Test

For the second test run, we used a Torrey Pines hotplate in SNSF, which was determined to be much more stable than the triple hotplate. We verified the temperature reading with an IR thermometer and it matched the temperature setting closely. Since the Torrey Pines hotplate has a reflective surface, we could not use the IR thermometer directly. Instead, we placed a black non-reflective metal piece on the hotplate and used this as a proxy for IR thermometry (see Fig. 16). Temperature was monitored throughout the reflow experiment to check for potential deviations from the set temperature.

For the second test, we used another sample at increasing temperatures (Table 2) with a 2 min reflow time for each temperature. Examples of optical images are shown in Figures 17 and 18.

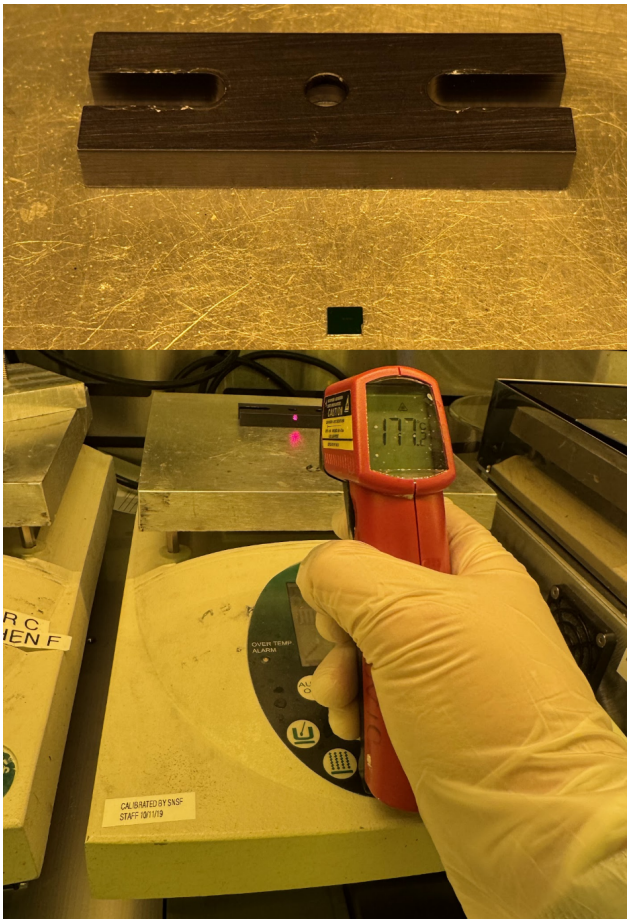


Figure 16: SNSF Torrey Pines hotplate.

Temp. setting	**Measured temp. (IR)**	**Observation (optical microscope)**
160 °C	155–160 °C	Significant reflow observed on all samples. Very prominent gradients on disks, and saw droplets of resists clumping due to surface tension.
170 °C	168–172 °C	Significant reflow observed on all samples. Waveguides start to clump together more. More pronounced difference in reflow dynamics for resonators at different doses. Smaller rings don't reflow as much as larger ones.
180 °C	178–181 °C	Collapsing features observed. Rings and waveguides melt/clump at multiple locations for all doses.

Table 2: Second reflow test temperature settings and observations

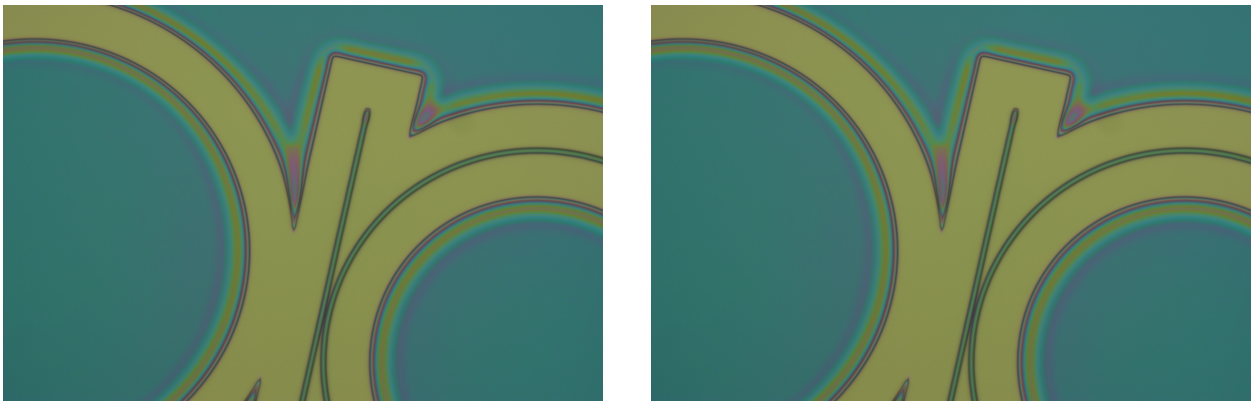


Figure 17: Second reflow test sample after heating at 160 °C, lowest dose (left) and highest dose (right).

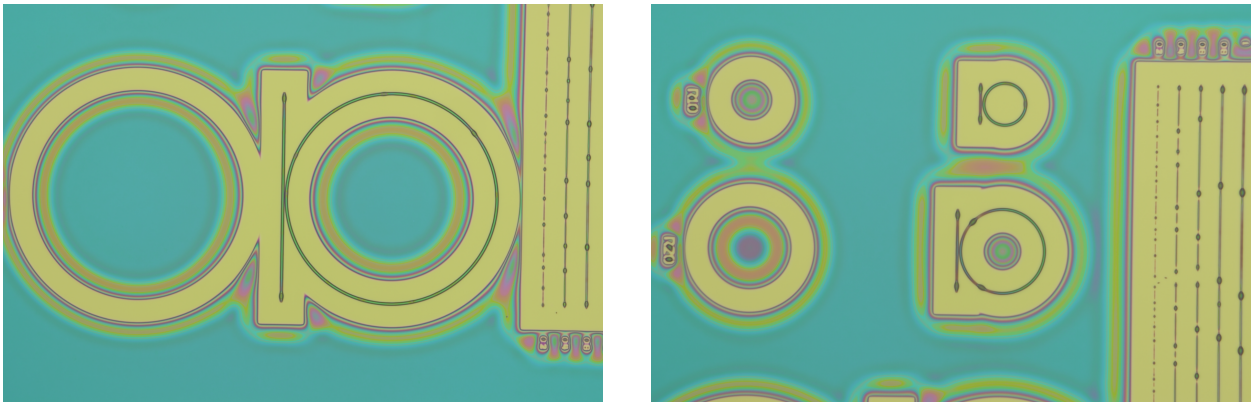


Figure 18: Second reflow test sample after heating at 180 °C, lowest dose (left) and highest dose (right).

5.3 Study of Reflow Temperature

Based on the results of the test runs, we decided to use the Torrey Pines hotplate to study how ZEP520A reflow dynamics depend on the temperature. Similar to the tests, reflow time was fixed at 2 minutes, followed by a 1-minute cool down on the metal surface of the bench. An IR thermometer was used to monitor the reflow process. As structural collapse was seen at temperatures above 160 °C in the second test run, we limited the reflow temperature experiment to six samples: Reference (no reflow), 120 °C, 130 °C, 140 °C, 150 °C, and 160 °C.

From optical microscope images (Fig. 19, Table 3), evidence of reflow can be seen from the colored fringes at the edges of the ZEP520A disks, which become visible around 130 °C. The colors are the result of thin-film interference as the ZEP520A structures change thickness near the edges, while the bulk structures retain the same color (thickness). The thinner waveguides become distorted due to ZEP520A flowing, and show visible clumps at temperatures higher than 150 °C. Based on the optical images, we can conclude that reflowing

ZEP520A for 2 minutes at temperatures between 120 °C – 140 °C preserves most of the optical structures, and no collapsing features are observed. However, more precise characterization tools, namely scanning electron microscopy (SEM) and atomic force microscopy (AFM), were used to verify the structural integrity of the devices.

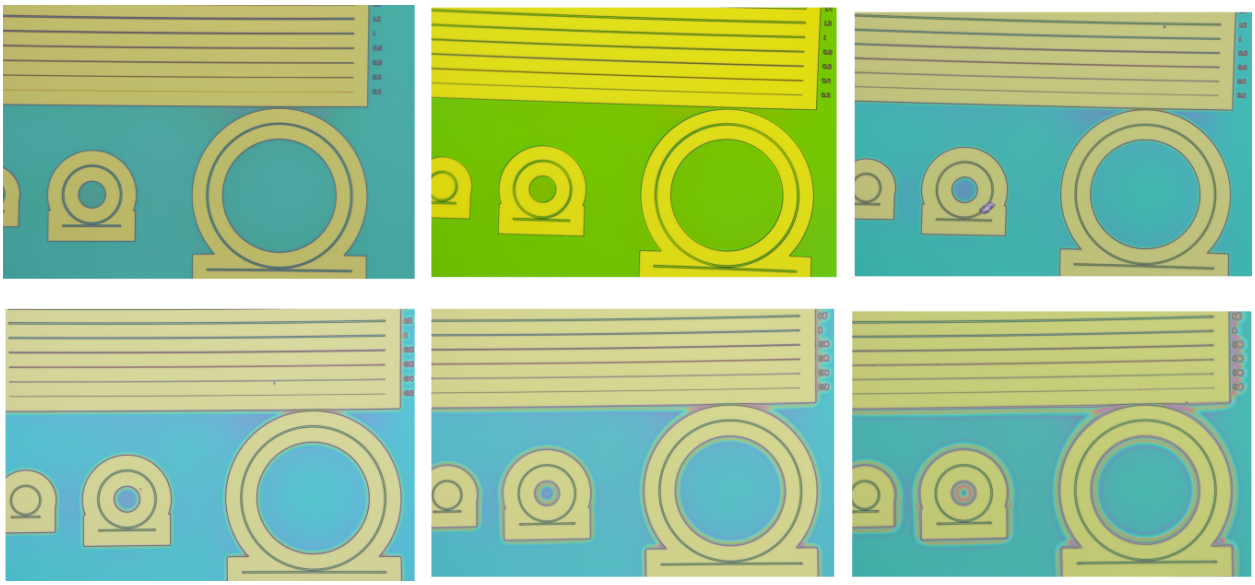


Figure 19: Reflow temperature experiment (optical microscope images). **Top, left to right**: Reference (no reflow), 120 °C, 130 °C. **Bottom, left to right**: 140 °C, 150 °C, 160 °C. All samples shown here were exposed at 250 µC/cm^2 in EBPG. The 120 °C image has a different color due to a different microscope filter.

Temp. (setting)	**Measured temp. (IR)**	**Observation (optical microscope)**
Reference	N/A	
120 °C	120–121 °C	Minimal color gradient on disks.
130 °C	128–131 °C	Some color gradient on disks. Narrow waveguides seem to be a different color (reddish).
140 °C	138–140 °C	More prominent color gradient. Ends of bus waveguides are bulb-shaped.
150 °C	148–150 °C	More prominent color gradient, especially for small disks. All waveguides have changed color (even the 3 µm waveguide is red).
160 °C	159–161 °C	Very prominent pink/orange boundary around all resist edges, labels starting to melt. Droplets starting to form for narrow waveguides (0.2–0.8 µm), no droplets for wide waveguides.

Table 3: Temperature settings and observations of the reflow temperature sweep experiment

6 SiN Etching

6.1 Dry Etching

After reflow, we transferred the resist pattern of the six samples to silicon nitride using SNF Oxford-RIE (reactive ion etcher). We followed the established SiN etch recipe by our lab group, which consists of two parts:

Chamber clean and season:

1. Pump to 5e-5
2. Repeat 2
3. Chamber clean (10 min, 50 sccm O_2, RF power 300 W, chamber pressure 100)
4. SiN season (5 min, 83 sccm CHF_3, 17 sccm CF_4, RF power 200 W, chamber pressure 30, helium backing 10)
5. Chamber clean (5 min)
6. SiN season (5 min)
7. Loop
8. Pump to 7e-5

SiN etch:

1. Pump to 5e-5
2. SiN etch (70 sccm CHF_3, 30 sccm CF_4, RF power 100 W, chamber pressure 30, helium backing 10)
3. Pump to 7e-5

From previous experience, Oxford-RIE etch rates tend to shift over time, so we performed a calibration etch on one dummy SiN-Si sample (thickness measured with SNF Filmetrics2) and one patterned ZEP-SiN-Si sample (thickness measured with SNF Filmetrics1, 100x objective), Fig. 20. This allowed us to determine the blanket (uniform film) etch rate as well as the patterned etch rate, which can be different for small features. For the calibration etch, we performed a 4-minute partial etch. The SiN thicknesses and etch rates were the following:

Blanket etch: Thickness before: 286.7 nm. Thickness after: 122.7 nm. Etch rate: **41.0 nm/min**

Patterned etch: Thickness before: 279.5 nm. Thickness after: 128.9 nm. Etch rate: **37.7 nm/min**

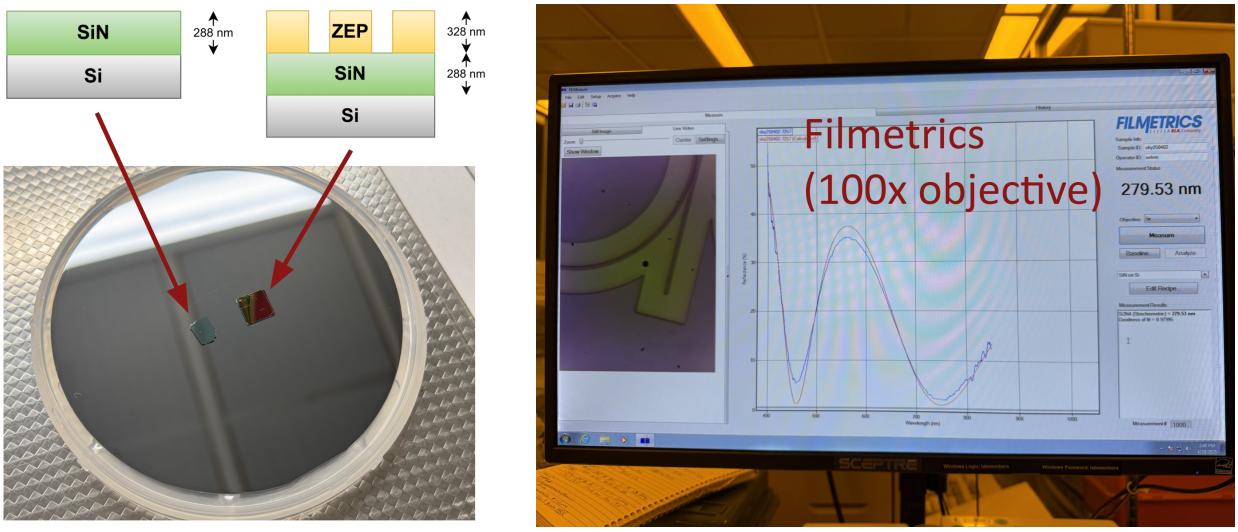


Figure 20: **Left:** SiN calibration etch. One sample is used to determine SiN blanket etch rate, while the other one is used to determine patterned SiN etch rate. **Right:** SNF Filmetrics, used to measure the thickness of patterned SiN before and after etching (100x objective).

Based on the calibration etch results, patterned etch is 8% slower than blanket etch, which implies the importance of considering this effect when determining etch rates for patterned devices.

For the reflowed devices, we performed a full etch through the SiN layer. To err on the side of overetching, we used the patterned etch rate (37.7 nm/min) and added 15% overetch margin to our etch time. Assuming SiN thickness of 291 nm, we determined an appropriate etch time for reflowed samples to be 8 min 53 s. Reflowed samples were then cleaned, seasoned, and etched under the same conditions as the calibration etch, with the only difference being the longer etch time.

During etching, samples were mounted on a Si carrier wafer using Santovac oil. Santovac oil was then cleaned from the backside of the chips with an acetone-soaked swab. The carrier wafer was cleaned with acetone and isopropanol spray and reused.

6.2 Resist Stripping

As plasma etching can burn the resist, its removal after etching can be challenging. For the resist stripping, we again used an established recipe in our lab group:

1. Soak in acetone (1 h)
2. Soak in Remover 1165 (3 h – overnight)
3. Clean in heated piranha solution (120 °C, 20 min, wbflexcorr-2)
4. Clean in 2% hydrofluoric acid, followed by 3 DI water dips.

As shown in Fig. 21, Remover 1165 removes most resist but struggles to strip resist near the device patterns. Acid clean (piranha, HF) generally cleans the resist well, although one of our samples (160 °C) still had some ZEP520A residue left even after the acid clean. An alternative method for removing resist could use O_2 plasma (SNF samco or matrix).

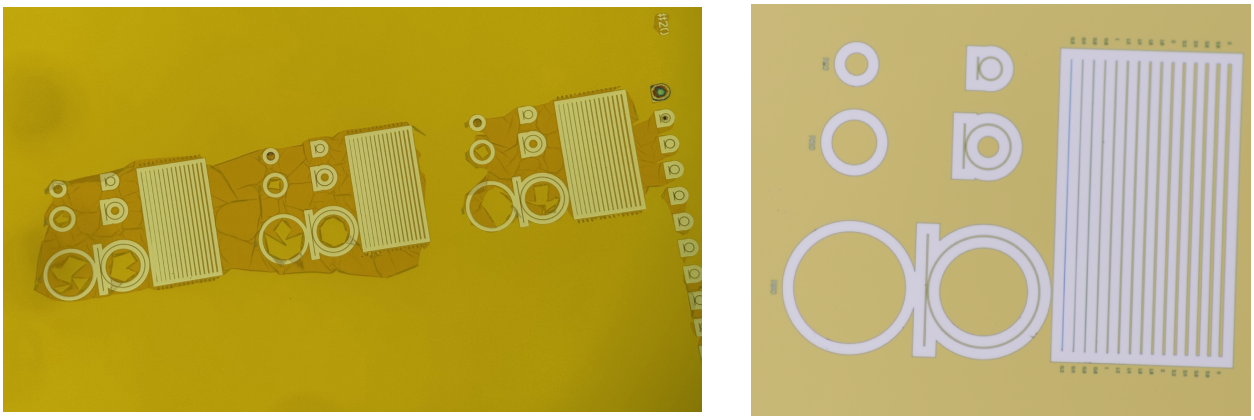


Figure 21: Example images of etched SiN devices after Remover 1165 clean (left) and after piranha/HF clean (right).

7 Characterization of ZEP520A Reflow

7.1 AFM Characterization

Profilometry: To verify surface roughness as well as devices profile after reflowing, we performed atomic force microscopy (AFM) characterization with Park NX-10 AFM in SNSF. We first measured the profile of the waveguide couplers (two 1.2 µm wide waveguides with a 0.4 µm gap in between) to study their structural integrity at various temperatures. Surprisingly, all couplers survived the 2-minute reflow, and the distance between the waveguides was preserved after reflow, as shown in Fig. 22. An explanation for this phenomenon can be attributed to ZEP520A surface tension. Rather than the resist melting and spreading out, ZEP520A instead reshapes itself into a dome-shaped like structure, even becoming taller during the reflow process. This happens for features with low enough aspect ratio, where the surface tension is stronger than the gravitational effects, thereby keeping the structures from collapsing.

It can also be seen that the dome-shaped profile is very similar for temperatures between 130 °C and 160 °C. For 120 °C, which is closer to glass transition temperature, the profile is closer to the reference device but still has round edges.

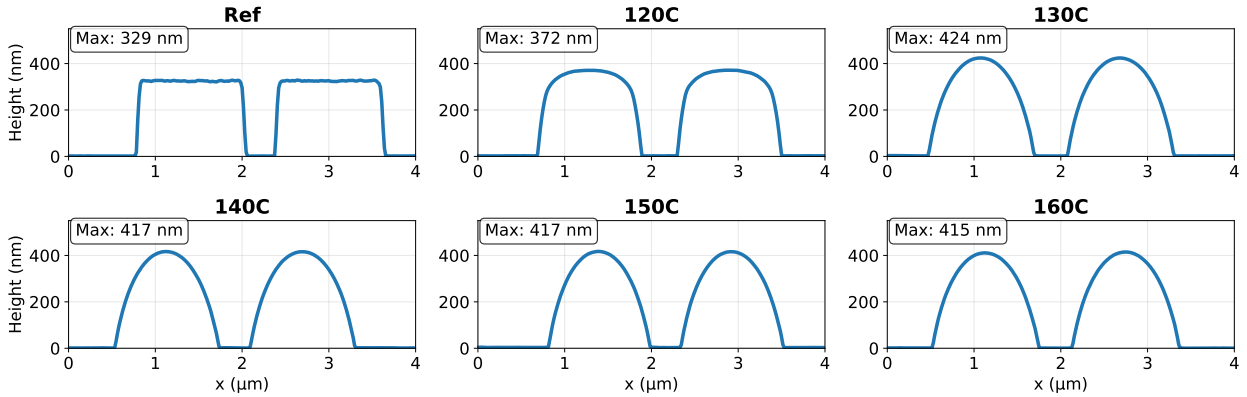


Figure 22: ZEP520A height profile at various reflow temperatures (waveguide coupler, measured with Park NX-10 AFM). Notice the coupler distance, ie the seperation between two waveguides, is preserved throughout the reflow.

The side profiles of the largest disk (50 µm radius) are shown in Fig. 23. Rather than the whole disk becoming dome-shaped, only the edge of the disk is affected during reflow. During the reflow process, the edge becomes smooth and an "ear" appears which becomes taller at higher temperatures.

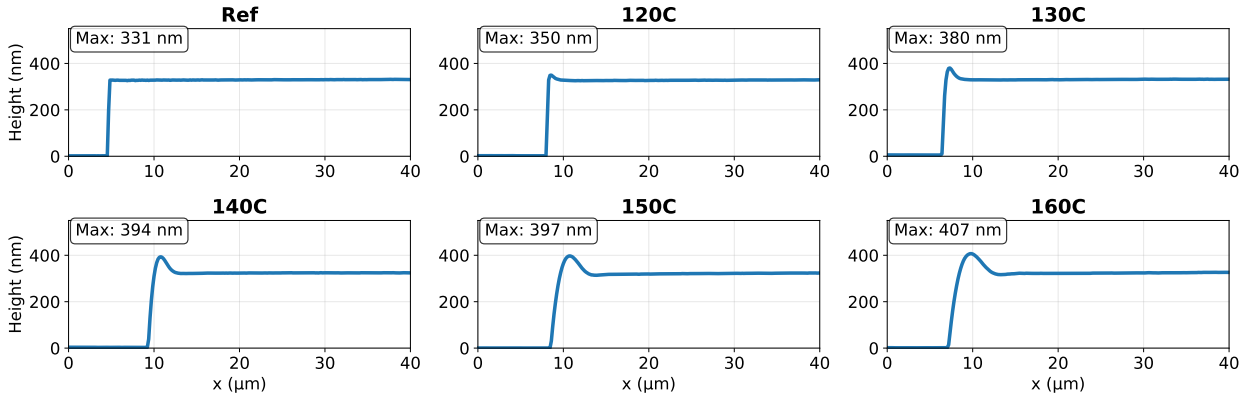


Figure 23: ZEP520A height profile at various reflow temperatures (50 µm radius disk, measured with Park NX-10 AFM).

Sidewall roughness and angle characterization: To compare sidewall roughness and angle at various temperatures, we took 1×1 µm images of the disk edge for all the samples (Fig. 24). The AFM images were flattened and rows aligned (median of differences) in post-processing using Gwyddion software. As can be seen from the blue line (average profile), the sidewall is smooth, curved, and becomes more slanted at higher temperatures. The purple line shows the angle of the sidewall at various positions, calculated from the gradient of the blue line.

To characterize sidewall roughness, we calculated the root-mean-square (RMS) roughness of vertical profiles (plotted orange). Calculating line roughnesses rather than surface roughnesses of masked areas allowed us to effectively quantify the roughness of curved surfaces. To account for slant and large correlation length waviness, the best-fit quadratic was subtracted from each profile before calculating RMS roughness.

In general, the reflowed resist is very smooth, with a typical roughness 200–300 pm, which is comparable to SiN inherent surface roughness. The spikes of roughness near the edge are mostly artefacts of our measurement, as the devices were not perfectly vertically aligned and mostly originate from large correlation length deviations. Numerical sidewall angle and roughness values are summarized in Section 9. While the reflowed samples have smooth sidewalls, we cannot make a conclusive comparison to the reference (no reflow) device, which has vertical sidewalls. For the reference sample, our measurement was limited by the cone angle of the AFM probe, so the measured sidewall roughness is meaningless, and the measured sidewall angle is a lower bound.

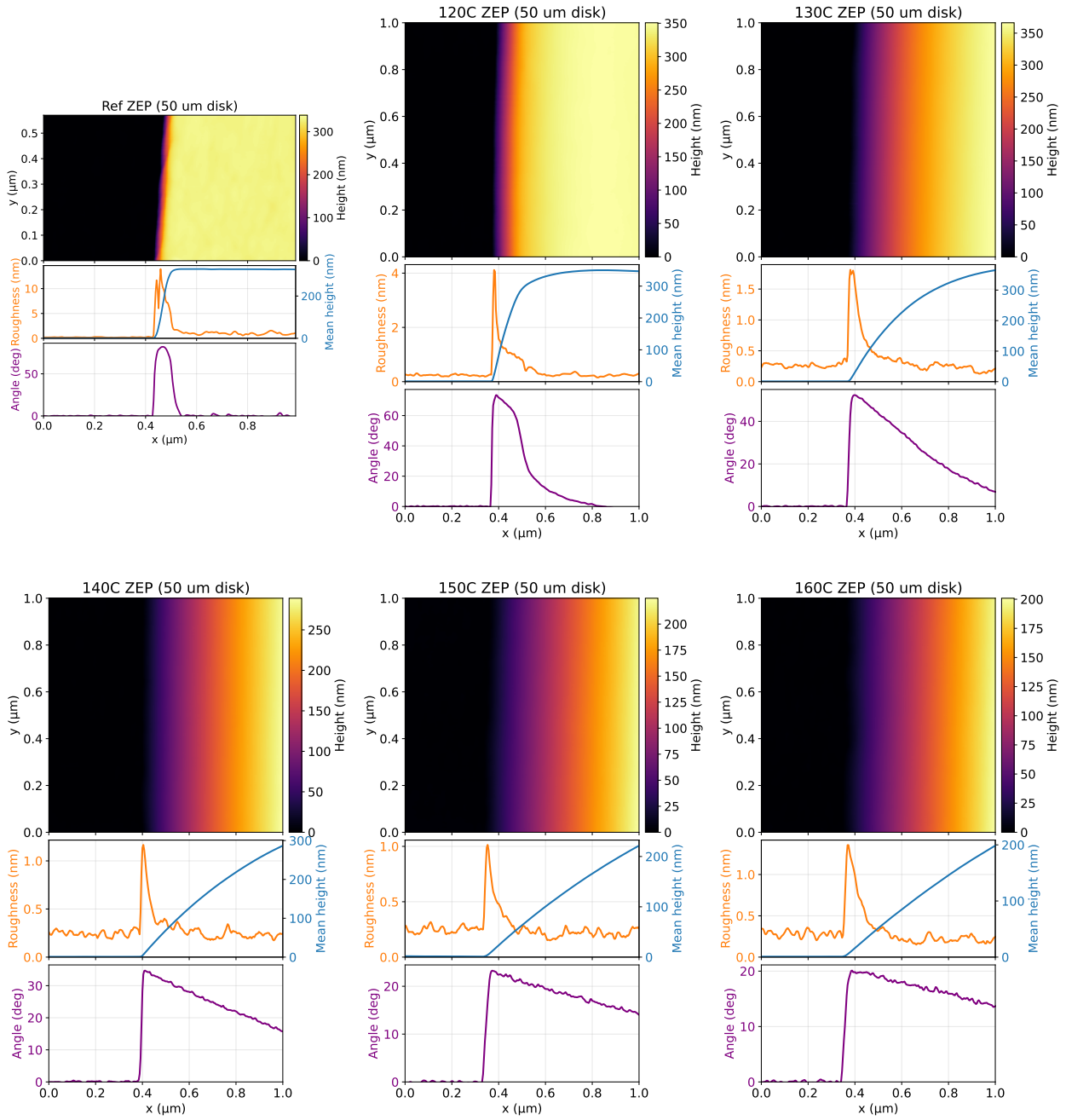


Figure 24: AFM height images of ZEP520A at various reflow temperatures (50 µm radius disk edge). The plots below show the average height, RMS roughness, and angle (gradient of average height) of vertical profiles.

For completeness, Fig. 25 shows a comparison of various structure images and profiles between the reference device and a sample from the second test run, reflowed up to 180 °C.

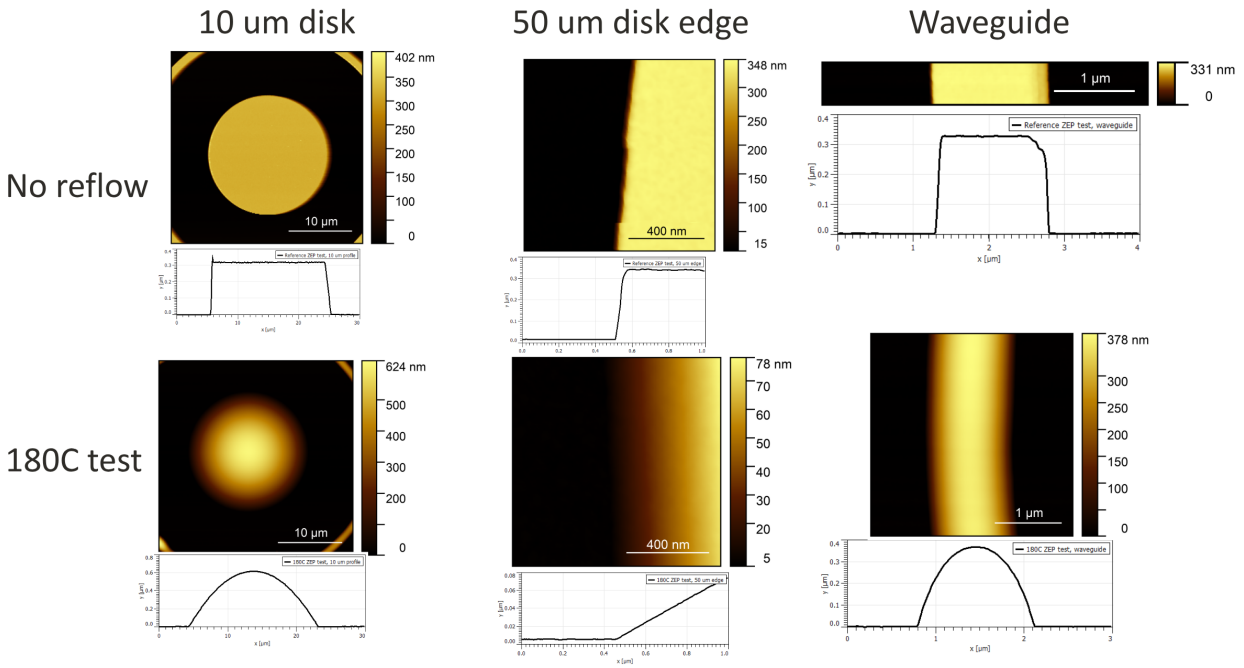


Figure 25: AFM height image of various structures, comparison between reference (no reflow) and second reflow test sample (180 °C).

7.2 SEM Characterization

To qualitatively compare the sidewall roughness of reference and reflowed devices, we used the Zeiss Gemini 560 Scanning Electron Microscope (SEM) in SNSF to get high-resolution images of the reflowed ZEP520A resist with a 45° mount to see the sidewalls.

However, for electron beam voltages of ∼1 kV and higher, charging effects would occur due to the low conductivity of the resist. As low-voltage imaging requires short working distance (4–5 mm) and the 45° mount limited us to working distances above 6 mm, we did not obtain high-quality images of the sidewalls (Fig. 26, right). For top-down imaging, where we could use a shorter working distance, we obtained a high-quality image with 0.5 kV voltage (left), but this was not helpful for determining sidewall roughness. Therefore, we opted to mainly rely on atomic force microscopy (AFM) for characterization.

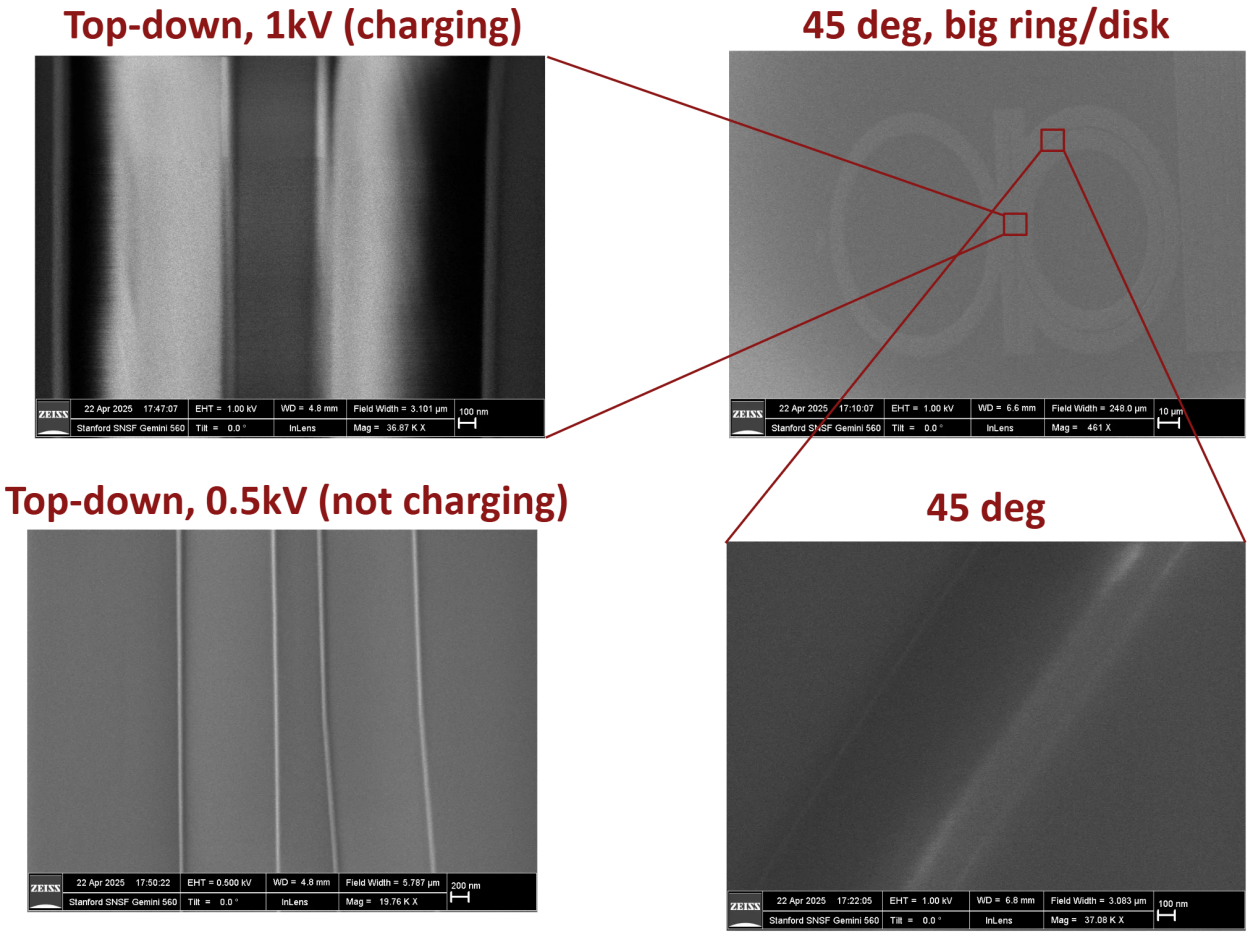


Figure 26: SEM images of patterned ZEP520A (reference device) at different voltages (0.5, 1 kV) and at two different mount angles (top-down, 45° mount).

7.3 Other Profilometric Tools

During device characterization, we also tested two other tools to measure profilometry: Dektak XT-S Stylus Profiler and Keyence VK-X250/260K 3D Laser Scanning Confocal Microscope in SNSF. While these tools are less accurate than SEM and AFM, they are much faster and easier to use.

However, both of these tools were unsuccessful in measuring accurate profiles. While the Dektak profilometer could resolve waveguides in the array (Fig. 27), the large stylus radius (12.5 µm) does not allow accurate measurement of small micron-level features. Keyence confocal microscope can, in principle, measure the height of details to nm-level accuracy; however, it also did not produce correct profile measurements (Fig. 28).

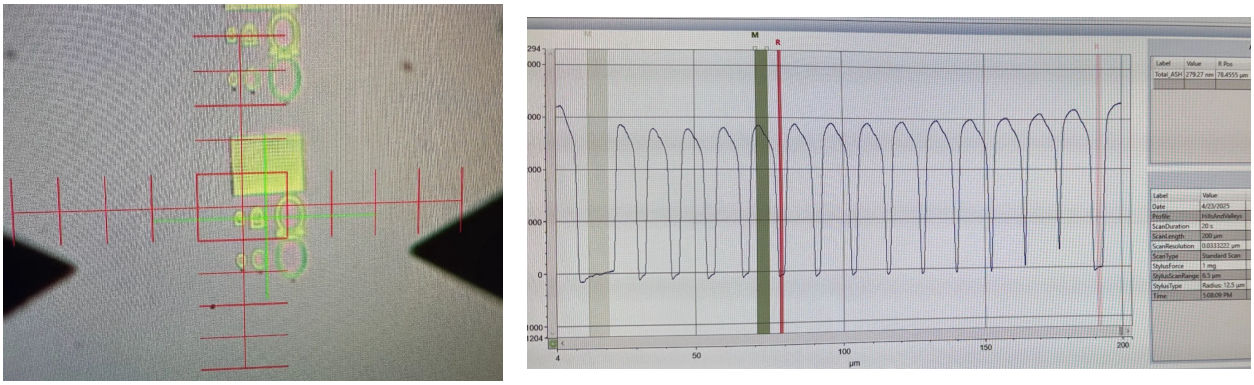


Figure 27: Dektak profilometer alignment (left) and measured profile of waveguides (right).

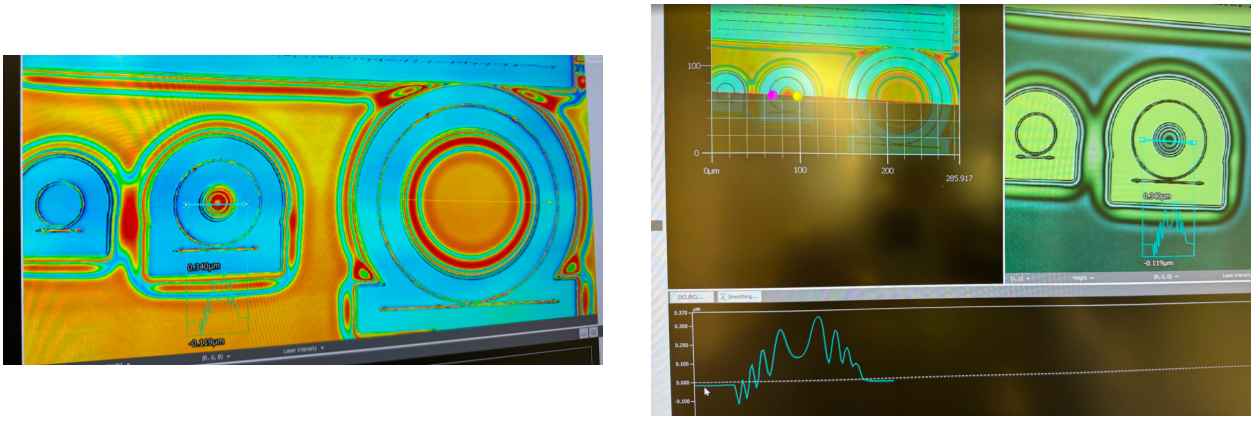


Figure 28: Keyence laser scanning confocal microscope heightmap (left) and measured profile of a 10 µm radius disk (ZEP520A, 180 °C reflow test).

8 Characterization of Etched SiN Devices

8.1 AFM Characterization

Profilometry: We characterized the profiles of SiN waveguide couplers after etching (Fig. 29), similar to Section 7.1. Surprisingly, the profiles show waveguides merging together at 120 °C and 130 °C, while becoming separated again at higher temperatures. One possible hypothesis is that at temperatures near the transition temperature, ZEP520A melts only partially, so spreads out. However, this does not agree with the findings in Fig. 22, where couplers at all temperatures remained unmerged. Therefore, we do not know the reason for this effect nor whether it is persistent between repeated experiments.

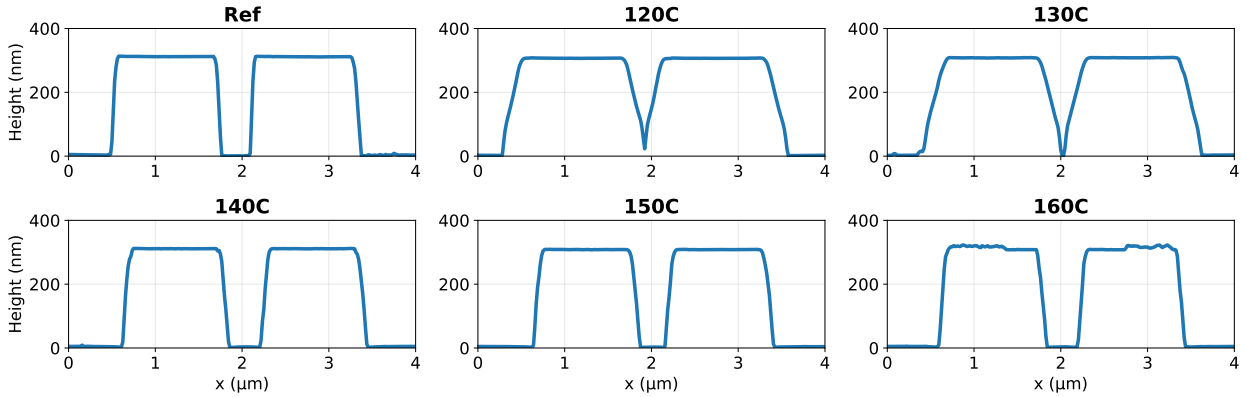


Figure 29: SiN height profile after etching at various reflow temperatures (waveguide coupler, measured with Park NX-10 AFM).

Sidewall roughness and angle characterization: Fig. 30 shows the AFM height images of etched SiN sidewalls, measured similarly as ZEP520A sidewalls in Section 7.1. Again, sidewalls become more slanted at higher reflow temperatures, agreeing with the trend of ZEP520A.

As opposed to smooth ZEP520A sidewalls with a typical roughness of 300 pm, etched SiN is much rougher (typical roughness 3 nm). We believe that the roughness is caused by bombardment of ions during dry etching and could indicate an unoptimal etch chemistry and/or too physical etch parameters. The sidewall roughness and angle values are summarized in Section 9.

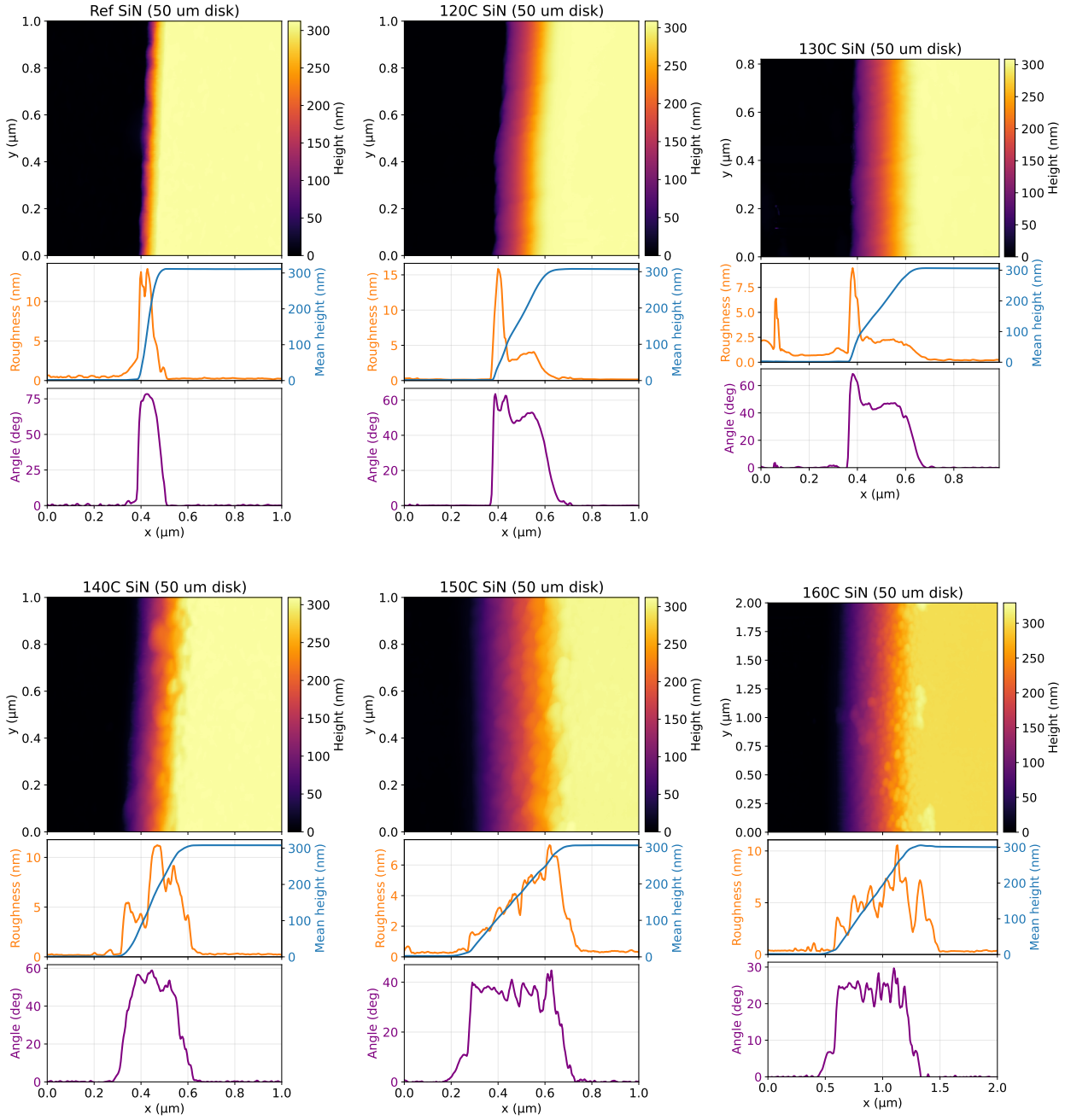


Figure 30: AFM height images of etched SiN at various reflow temperatures (50 µm radius disk edge). The plots below show the average height, RMS roughness, and angle (gradient of average height) of vertical profiles.

8.2 SEM Characterization

Examples of SEM images of etched SiN devices (45° mount) are shown in Fig. 31. The optimal imaging conditions appeared to be 2 kV with 60 µm aperture. At lower voltages, the image quality would be reduced due to a high working distance. Charging effects intermittently appeared, which limited the image quality, especially at higher voltages.

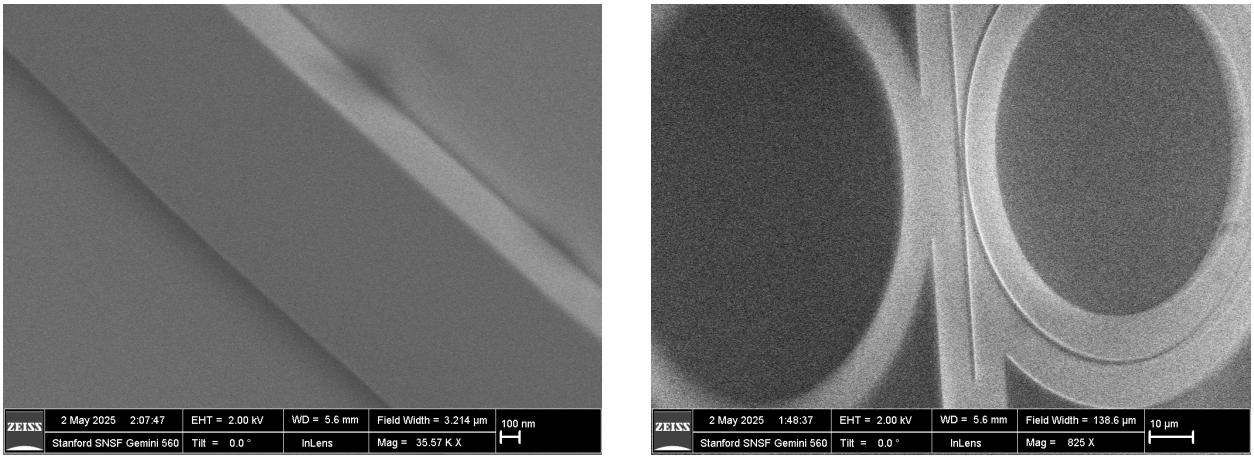


Figure 31: SEM images of an etched SiN device (reference, no reflow).

Although the SEM image quality was higher for etched SiN than for ZEP520A, it was still challenging to see high-resolution details such as sidewall roughness. Some sidewall roughness was initially visible for the reference and 120 °C devices (Fig. 32). However, this observation was not persistent and disappeared later with similar imaging conditions. Therefore, we could not use the regular InLens imaging mode to make conclusions about whether reflow improves device sidewall roughness.

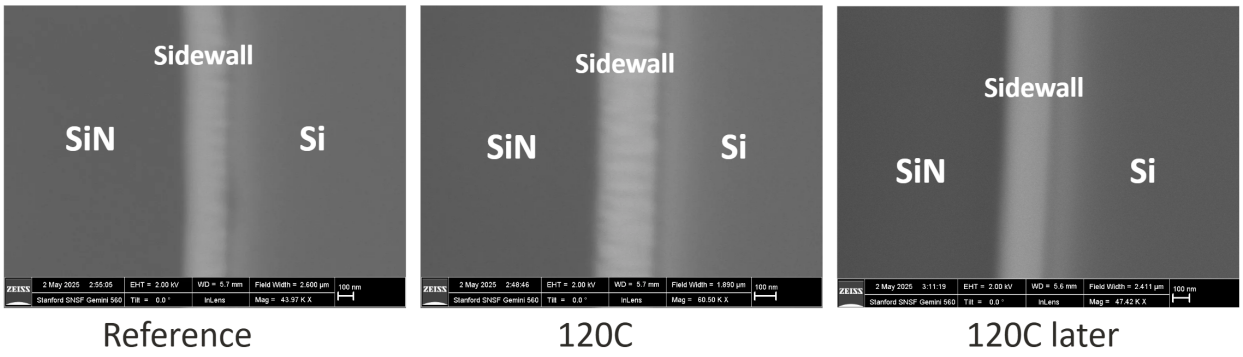


Figure 32: SEM images of a 50 µm disk sidewall edge (ref, 120 °C).

Nevertheless, we managed to get high-quality images with the SE imaging mode, where the electron detector is off-axis. The image (Fig. 33) shows significant sidewall and some surface roughness on the reference device. To mitigate charging effects of the sample, we sputter-coated a 2.3 nm layer of Au/Pd alloy on the devices. Due to time constraints, we were unable to take comparison images of the reflowed samples.

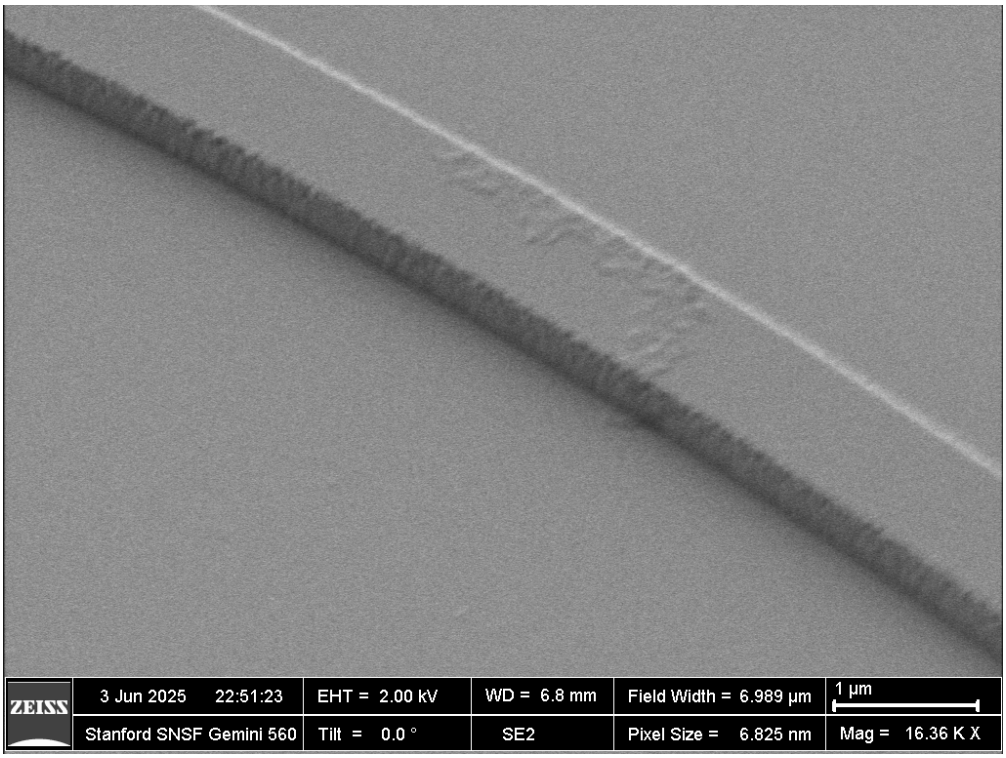


Figure 33: SEM image (SE imaging mode) of reference device SiN ring resonator waveguide (250 µC/cm^2 dose) at 2 kV and 30 µm aperture.

8.3 SEM with Charge Dissipation Layers

To mitigate charging issues and possibly improve SEM imaging quality, we tried spin-coating two different charge dissipation layers on the etched devices: Electra 92 and Discharge H2O X2. The benefit of charge dissipation layers over sputter coating is that they do not affect surface roughness, a metric we were trying to measure. Charge dissipation layers are also easier to remove than a metal coating. For this process, we used the following recipes:

Electra 92:

1. Dehydration bake at 150 °C for 2 min, cool down 1 min.
2. Spin coat Electra 92 at 3000 RPM, 60 s.
3. Bake at 90 °C for 2 min, cool down 1 min.
4. For removal: soak in DI water for 60 s.

Discharge H2O X2:

1. Dehydration bake at 150 °C for 10 min, cool down 1 min.
2. Spin coat Discharge H2O at 3000 RPM, 60 s.
3. Leave to dry in ambient air for 5 min.

4. For removal: soak in DI water for 60 s.

However, neither of the methods worked well for us. Both charge dissipation layers had issues with adhesion to SiN samples, even after a long dehydration bake (Fig. 34). This might have occurred because charge dissipation layers are designed to be spin coated on electron beam resists, not on silicon-based materials.

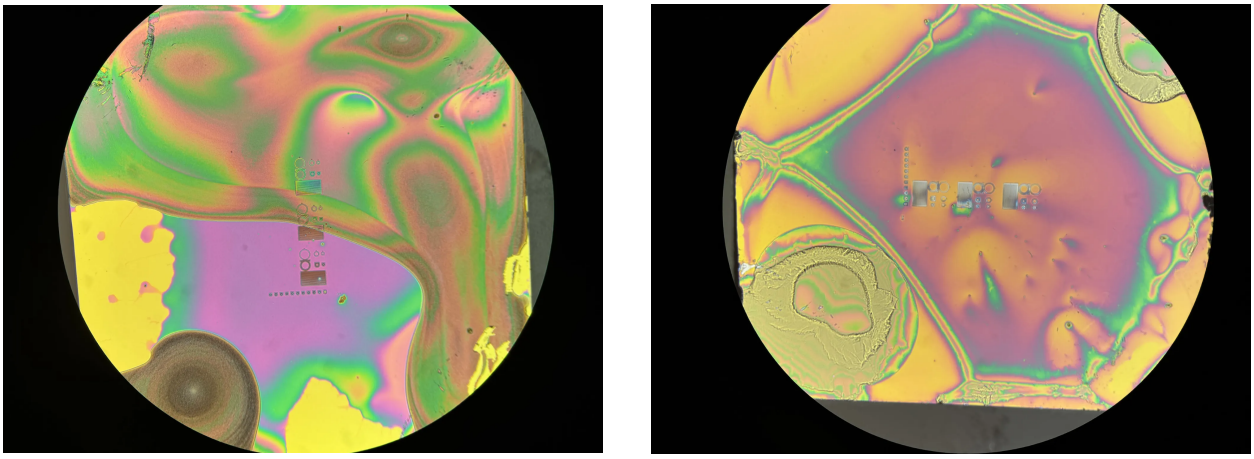


Figure 34: Spin-coated charge dissipation layers: Electra 92 (left) and Discharge H2O X2 (right). Due to imperfect adhesion, the layers are non-uniform.

As the dissipation layer still mostly covered the devices, we tried SEM imaging with both layers. For Electra 92, we did not see the devices at all. For Discharge H2O, we saw the devices, but the charging issues were significantly worse than without the layer (Fig. 35). As a result, we decided to opt for Au/Pd sputtering to improve image quality (see SE image above).

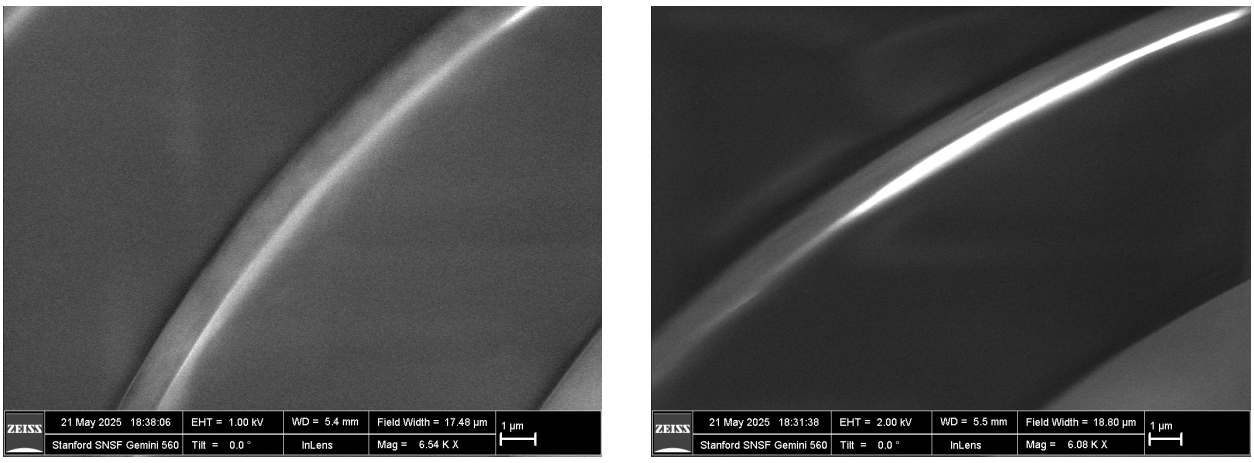


Figure 35: SEM images of etched SiN devices with Discharge H2O charge dissipation layer. (120 °C, waveguide, 1 and 2 kV)

9 Results

Table 4 summarizes the sidewall roughness and angle of devices (50 µm radius disk) reflowed at various temperatures, measured using atomic force microscopy. The sidewall roughness was calculated as the average vertical profile roughness (Figures 24 and 30) for which the mean height of the vertical profile was between the 25th and 75th percentile. For ZEP profiles (smooth, but varying slope), the sidewall angle was calculated as the maximum gradient of the mean height. For SiN profiles (rough, but approximately constant slope), the sidewall angle was calculated as the average gradient where the mean height was between the 25th and 75th percentile.

It should be noted that these values, especially the sidewall angle, depend on the feature size. While the profile of a large feature such as a 50 µm disk changes in the full 120–160 °C temperature range (Fig. 23), waveguide coupler profile remains similar at temperatures above 130 °C (Fig. 22). We still believe, however, that the general trend of values in Table 4 generalizes to features with various sizes. We could not deduce sidewall roughness for the reference device as the AFM probe was unable to accurately measure vertical features.

Temperature	**ZEP sidewall roughness (nm)**	**SiN sidewall roughness (nm)**	**ZEP sidewall angle (deg)**	**SiN sidewall angle (deg)**
Reference	-	-	>82	>77
120 °C	1.14	3.64	74	52
130 °C	0.37	2.36	52	46
140 °C	0.26	7.64	35	53
150 °C	0.22	3.75	23	36
160 °C	0.23	5.35	20	24
Avg. roughness	**0.45**	**4.55**		

Table 4: Sidewall roughness and angle measurements for ZEP520A and etched SiN at different reflow temperatures (50 µm radius disk edge).

10 Conclusion

In this project, we studied the thermal reflow of ZEP520A at various temperatures (120–160 °C) and characterized the properties of both reflowed resist and etched SiN devices.

We demonstrated the feasibility of reflowing ZEP520A to produce near-atomically smooth resist surfaces, with typical sidewall roughness of 200–300 pm, potentially allowing fabrication of high-Q photonic resonators. We showed that the structural integrity of devices, including waveguide couplers with a 400 nm gap, was preserved at all temperatures. As expected from the literature, sidewalls become more slanted at higher reflow temperatures, with the sidewall angle monotonically decreasing from 74° to 20° when increasing temperature from 120 °C to 160 °C (50 µm radius disk).

However, dry etching SiN introduced significant roughness in the devices, increasing sidewall roughness approximately 10 times and negating the benefits of resist reflow. Therefore, future work could include optimization of SiN etch chemistry and power to reduce etch-induced roughness.

While we saw improvements in ZEP520A top surface roughness during reflow, we cannot yet make a conclusive comparison of sidewall roughness before and after reflow, as regular AFM probes cannot image vertical sidewalls. However, we demonstrated that the SE imaging mode in Gemini SEM shows finer features, which could enable comparison with reference devices. Quantitative comparisons could also be made with a tilted AFM mount.

11 Outlook

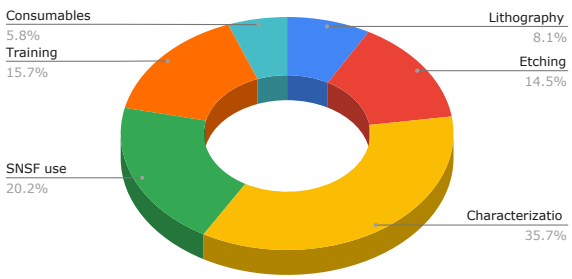
Given the feasible nature of ZEP520A reflow and its wide compatibility with many photonic materials such as Si, SiN, SiC, GaAs, AlGaAs, diamond, and sapphire, we envision that our reflow process could also be carried out with the aforementioned materials. This will enable the fabrication of ultra-high Q ($> 10^6$, potentially $> 10^7$) photonic microresonators by smoothening the surface and sidewalls, thereby reducing scattering loss. For materials such as SiC, sapphire, and diamond, which have a relatively low etch selectivity with ZEP520A, we could introduce a hard mask process with aluminium oxide or ruthenium, where the reflowed ZEP520A patterns can be transferred into the hard mask and then from the hard mask into the substrate. While reflow has been shown to perform well with hard mask (oxide hard mask [6] and SiN hard mask [7]) for AlGaAs, future work could study if such transfer can be succesful with aluminium oxide or ruthenium.

To study how well patterns can be transferred from resist to hard mask, etch chemistry will be the main contributing factor. Again, given that the limiting factor of roughness is etching, it seems to be more important to focus on improving etch chemistry rather than reflow parameters. For the future study, we would like to develop chemistry for etching aluminium oxide or ruthenium with ZEP520A, Aluminium oxide hard mask has been successfully used by our lab group to etch diamond. Ruthenium hard masks, on the other hand, have not been extensively used in SNF, but a mixture of Cl_2/O_2 has been demonstrated to produce volatile RuO_4 as a result [8].

12 Budget

Total spending: **$3569.83**

Category	Item	Spent	
Lithography	E-beam patterning (EBPG)	$290.40	
Etching	Etching (Ox-RIE)	$395.28	
	Wet bench (wbflexcorr-2)	$59.73	
	Resist stripping (samco)	$63.51	
Characterization	AFM (Park NX-10)	$456.66	
	AFM probes	$160.00	
	SEM (Gemini)	$623.33	
	Sputter coating (Cressington)	$14.50	
	Profilometry (Dektak, Keyence)	$16.00	
	Thickness measurement (Filmetrics)	$4.00	
SNSF use	SNSF daily use	$720.00	(approx.)
Training	AFM training	$313.75	
	SEM training	$136.67	
	Ox-RIE training	$110.00	
Consumables	Consumables (wafers, containers)	$206.00	
	Total:	**$3,569.83**	



13 Acknowledgments

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References

[1] Kerry Allan Wilson and Frank Vollmer. *Whispering Gallery Mode Resonator Biosensors*, page 4387–4401. Springer Netherlands, 2016.

[2] Matthew W. Puckett, Kaikai Liu, Nitesh Chauhan, Qiancheng Zhao, Naijun Jin, Haotian Cheng, Jianfeng Wu, Ryan O. Behunin, Peter T. Rakich, Karl D. Nelson, and Daniel J. Blumenthal. 422 million intrinsic quality factor planar integrated all-waveguide resonator with sub-mhz linewidth. *Nature Communications*, 12(1), February 2021.

[3] Daniil M. Lukin, Bennet Windt, Miguel Bello, Dominic Catanzaro, Melissa A. Guidry, Eran Lustig, Souvik Biswas, Giovanni Scuri, Trung Kien Le, Joshua Yang, Arina A. Nikitina, Misagh Ghezellou, Hiroshi Abe, Takeshi Ohshima, Jawad Ul-Hassan, and Jelena Vučković. Mesoscopic cavity quantum electrodynamics with phase-disordered emitters in a kerr nonlinear resonator, 2025.

[4] Rodrigo Benevides, Michaël Ménard, Gustavo S. Wiederhecker, and Thiago P. Mayer Alegre. Ar/cl2 etching of gaas optomechanical microdisks fabricated with positive electroresist. *Optical Materials Express*, 10(1):57, December 2019.

[5] R. Kirchner, V.A. Guzenko, I. Vartiainen, N. Chidambaram, and H. Schift. Zep520a — a resist for electron-beam grayscale lithography and thermal reflow. *Microelectronic Engineering*, 153:71–76, March 2016.

[6] Weiqiang Xie, Lin Chang, Haowen Shu, Justin C. Norman, Jon D. Peters, Xingjun Wang, and John E. Bowers. Ultrahigh-q algaas-on-insulator microresonators for integrated nonlinear photonics. *Optics Express*, 28(22):32894, October 2020.

[7] Yuqian Zhang, Changzheng Sun, Bing Xiong, Jian Wang, Zhibiao Hao, Lai Wang, Yanjun Han, Hongtao Li, and Yi Luo. Suspended algaas-integrated nonlinear photonics, 2023.

[8] Masaya Imai, Miyako Matsui, Ryoko Sugano, Takashi Shiota, Ko-ichi Takasaki, Makoto Miura, Yohei Ishii, and Kenichi Kuwahara. Activation mechanism of ruthenium etching by cl-based radicals in o2/cl2 plasma. *Japanese Journal of Applied Physics*, 62(SI):SI1014, May 2023.