

Optimization of TiN Microheaters

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Titanium Nitride (TiN) microheaters show promise for a variety of applications including mid-IR emitters for gas sensing and resonant catalysis of various chemical reactions. However, typical deposition recipes for TiN in the SNF result in highly resistive and unstable films. This project achieves deposition of high-quality TiN films with resistivities approaching the best literature values for PVD TiN. Further testing on lithographic patterning and etching of these films is also presented. Finally, initial characterization of the microheaters is discussed.

CONTENTS

I. Motivation	3
A. Microheaters	3
B. TiN	3
C. Benifits to SNF community	3
II. Deposition Optimization	4
A. Process Flow	4
B. Pre-deposition Process	4
C. Critical Parameters and DoE	4
D. Final Optimization	5
E. Film Characterization	6
III. Film Processing	8
A. Lithography	8
B. Etching Optimization	10
IV. Device Fabrication	12
A. Process Flow	12
B. Fabricated Devices	14
V. Device Characterization	15
A. Emissivity Testing	15
B. Resistivity measurements	17
C. Pulsed Measurements	17
VI. Conclusions and Future Work	19
VII. Budget	20
VIII. Acknowledgements	20
A. Etching DoE Results	21
References	21

I. MOTIVATION

A. Microheaters

People have been using heaters to precisely control temperature for years. Recently, microheaters are attracting more and more attention. The microheater is a micro system generating heat by Joule heating, ultrasonic heating, microwave heating, and more. The micro size means low thermal mass and low energy consumption, which allows microheaters to achieve fast thermal response and high temperature peaks.

Microheaters are widely used in medical devices, microelectromechanical systems (MEMS), wearable electronics, fuel cells, and more. One important application of microheaters is gas sensors. Gas sensors detect gas components by their absorption spectra. According to the Stefan-Boltzmann law, the radiation intensity increases as the temperature goes up. In this way, the microheaters can work as an excellent infrared (IR) radiation source as microheaters can reach high temperatures.

B. TiN

Choosing proper materials is key to fabricate gas sensors with high performance. Ideal heating materials should have high thermal stability, high thermal conductivity, a low coefficient of thermal expansion, and be compatible with complementary metal-oxide semiconductor (CMOS) fabrication processes.

Common heating materials used for gas sensors include aluminium and noble metals like gold and platinum. However, aluminium has a low melting point at 660°C. It's easily oxidized in air at medium temperatures which increases its resistance. Noble metals like gold and platinum were then explored. Though gold has a higher melting point at 1064 °C, it has poor adhesion with substrate materials. Platinum is another choice with even higher melting point at 1768 °C, but the resistivity of platinum starts to drift above 650 °C. Also, it has a large positive temperature coefficient of resistance (TCR), which means the heat will further accumulate at the hot points which decreases the long term stability.

Titanium nitride (TiN) is promising materials for thermal applications, as its melting point is as high as 2947 °C. Also TiN has relatively low resistivity and moderate thermal conductivity. TiN can be deposited through sputtering and atomic layer deposition (ALD), and further is a CMOS compatible material. Furthermore, its optical and electrical properties can be manipulated by controlling the stoichiometric ratio of Ti and N. In this way, TiN is a promising material for thermal, optical, and electrical applications.

C. Benefits to SNF community

This work benefits SNF researchers in multiple aspects:

1. We developed a recipe for high quality TiN deposition using the TiN target in Lesker2, which has a low resistivity approaching the limits of films deposited by physical vapor deposition (PVD).
2. We demonstrate methods to characterize TiN thin film quality and gather experiment results about the TiN properties.
3. We optimized a recipe for selectively etching TiN on SiN_x using PT-MTL.

4. We designed a process to fabricate microheaters and as well as test setups for related device characterization.

II. DEPOSITION OPTIMIZATION

A. Process Flow

Our deposition process broadly adheres to the following steps:

1. Clean the Si wafer following Radio American Corporation (RCA) cleaning procedure.
2. Use High Density Plasma Enhanced Chemical Vapor Deposition (HDPE CVD) to deposit a SiN_x layer of about 100nm for electrical insulation from the substrate,
3. Load the substrate into *lesker2* and perform a Ti getter for 4 minutes.
4. Bake the substrate and main chamber at 200 °C for 30min.
5. Perform a Ti getter again for 4 minutes.
6. Perform TiN sputtering under the desired conditions.

B. Pre-deposition Process

Si, SiO_2 and SiN_x wafers are often used as microheater substrates due to their high thermal conductivity. Here we chose Si as our substrate as it's transparent in mid IR wavelength which benefits our gas sensor application. We fetched 4 inch C-test <100> Si wafers for fabrication and cleaned it following the RCA cleaning procedure:

1. Removal of insoluble organic contaminants with a 5:1:1 $\text{H}_2\text{O} : \text{H}_2\text{O}_2 : \text{NH}_4\text{OH}$ solution.
2. Removal of a thin silicon dioxide layer where metallic contaminants may accumulate as a result of (1), using a diluted 50:1 $\text{H}_2\text{O}:\text{HF}$ solution.
3. Removal of ionic and heavy metal atomic contaminants using a solution of 6:1:1 $\text{H}_2\text{O} : \text{H}_2\text{O}_2 : \text{HCl}$ (SC-2).

RCA cleaning aimed to remove the surface contamination. After that an SiN_x layer was deposited onto the substrate using the PE-CVD tool *ccp-dep*, with the classical SNF receipt at 350 °C. An approximately 100 nm SiN_x thickness was deposited as the insulation layer.

C. Critical Parameters and DoE

For TiN deposition, *lesker2* is used. Before sputtering TiN, there are a few of steps to improve the TiN deposition quality.

First a 4 minute Ti getter sputtering at 5 mTorr is performed. The sputtering power is set at 200 W of direct current (DC). The Ti getter procedure does not deposit on the substrate as the shutter is closed. It should to decrease the base pressure by gettering any residual oxygen and other contaminants. The base pressure of the main chamber is how much gas is left after the previous user finished sputtering. Usually the main chamber base pressure of *lesker2* is as low as $1 * 10^{-8}$ Torr.

Following that, we bake the substrate at 200 °C for 30 minutes at ramping speed 10 °C/minute. Aftr that, we let it cool down naturally, which took about 40 minutes. Baking helps remove adsorbed oxygen and potential organics.

After baking, the Ti getter was performed again with the same setup. Because the chamber was vented again during baking, the base pressure might have increased.

Finally, it comes to TiN sputtering. The TiN is sputtered under 200 W DC power for 30 min. Other than that, there are four parameters might influence the deposition quality: substrate bias, substrate temperature, N_2 ratio and chamber pressure. Substrate bias was maintained by applying negative voltage onto the substrate. It prevents contaminants adsorption and burial. Substrate temperature is related with the deposition speed, film roughness, grain size, etc. The N_2 ratio is important when doing TiN reactive sputtering, however here we directly sputtered TiN by using TiN target. The N_2 might not influence that much here. Working pressure matters with the deposition rate.

To figure out how these four parameters matter here and further develop a high quality TiN, a Design-of-experiments (DoE) matrix was designed as Table I. There were nine unique conditions combined to see each parameter's effect. The specific values of each parameters were picked by experience.

To evaluate the quality of the TiN film, the film sheet resistivity was measured by an Ossila four-point probe system. The lower resistivity, the better quality we got. It is because the lower resistivity indicates higher carrier concentration, which can emit more IR light as the emissivity is higher. Also, the emission peak is narrower with a lower resistivity, which means it can be used as a single wavelength light source.

TABLE I: DoE matrix of unique TiN sputtering conditions

DoE#	Substrate Bias (W)	Temperature (C)	N_2 Flow (%)	Pressure (mTorr)	Thickness (nm)	Sheet Resistance (Ω /square)	Resistivity ($\mu\Omega\cdot m$)
1	0	200	0	2	14	360	5.04
2	25	27	0	8	45	28	1.26
3	0	27	8	8	83	14e3	116.2
4	25	200	8	8	35	28	0.99
5	0	27	8	2	58	198	11.5
6	25	27	0	2	51	20	1.02
7	25	200	8	2	39	22	0.86
8	0	200	0	8	86	670	57.6
9	0	27	0	2	82	58	4.76

D. Final Optimization

After spending several weeks on sputtering, the DoE matrix was finished with corresponding thin film resistivity. The result was analysed by JMP to figure out the weights of each parameters as shown in Fig. 1.

The substrate bias shows a large positive effect in decreasing resistivity. Increasing substrate temperature also helps decreasing resistivity. The N_2 ratio somehow increases the resistivity and decreases the film quality. Chamber pressure doesn't influence the result very much.

To further improve the TiN quality, TiN sputtering at different temperatures was explored with results in Fig. 2 a). This time the other variables were settled, with substrate bias at

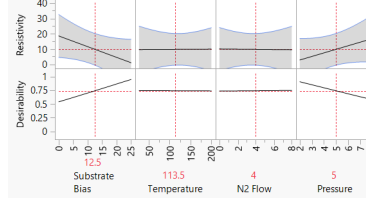


FIG. 1: JMP analysis of impact of each parameter on film resistivity.

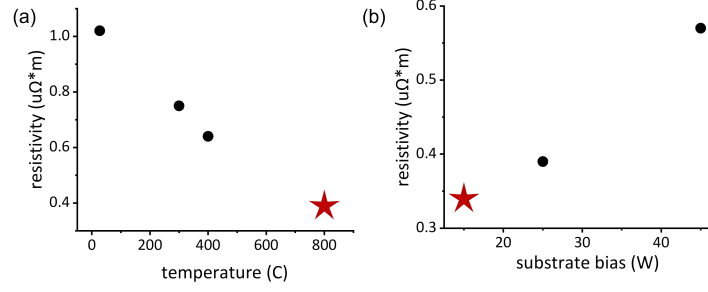


FIG. 2: Resistivity of TiN film sputtered under (a) various temperature with 25 W bias, 0 % N_2 and 2 mTorr working pressure (5 mTorr for 800 °C condition); (b) various substrate bias with 800 °C, 0 % rmN_2 and 5 mTorr working pressure

25 W, N_2 ratio at 0%, and pressure at 2 mTorr. As we expected, the resistivity decreases as the temperature increases. Then a sputtering at the highest temperature (800 °C) of *lesker2* was performed, in order to save time and budget. And it shows that the resistivity keep decreasing as temperature increases. When temperature reaches 800 °C, at 2 mTorr working pressure, the plasma failed to ignite. Thus, the working pressure was increased to 5 mTorr at 800 °C.

Finally, substrate biases were applied as in Fig. 2 b). Applying substrate bias did increase the film quality a lot compared to those without substrate bias. However, when comparing the samples with different bias, it shows that the resistivity increases as the bias increases. By applying substrate bias, the surface roughness decreases first as bias provides extra energy to form dense crystals, then the roughness increases as the bias increases, as the atom diffusion becomes more directional. Also the substrate bias prevents the surface oxidation at the beginning but improves the oxidation as the bias keeps increasing. These two factors explained why the substrate bias increasing lowers the film quality.

E. Film Characterization

Our best TiN was deposited under 15 W substrate bias, 800 °C substrate temperature, 0 % rmN_2 ratio and 5 mTorr working pressure. The lowest resistivity was $34 \mu\Omega\cdot\text{cm}$, which reaches the limit of PVD films. The film thickness was 44nm. The film was further characterized by X-ray diffraction (XRD) and X-ray photo-electron spectroscopy (XPS).

XPert was used for XRD as shown in Fig. 3. XRD was perform in grazing incident (GI) mode to avoid the disruption of Si. The result curve matched with classic face center cubic (FCC) characteristic peaks, as TiN has an FCC lattice. It proved that we got TiN crystals. The size of sub-micrometre crystallites of (1 1 1) face was at 12 nm, calculated by Scherrer

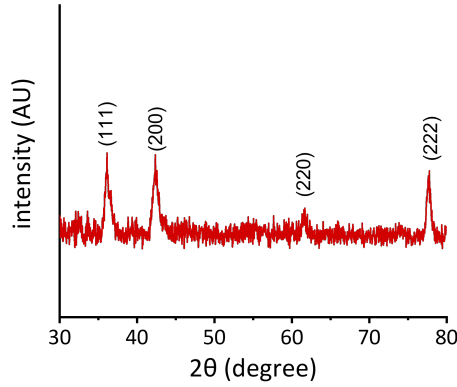


FIG. 3: GI-XRD results of the TiN sputtered under 800 °C and 15 W substrate bias, the ϕ angle was set to 40 ° to avoid silicon's disruption

equation.

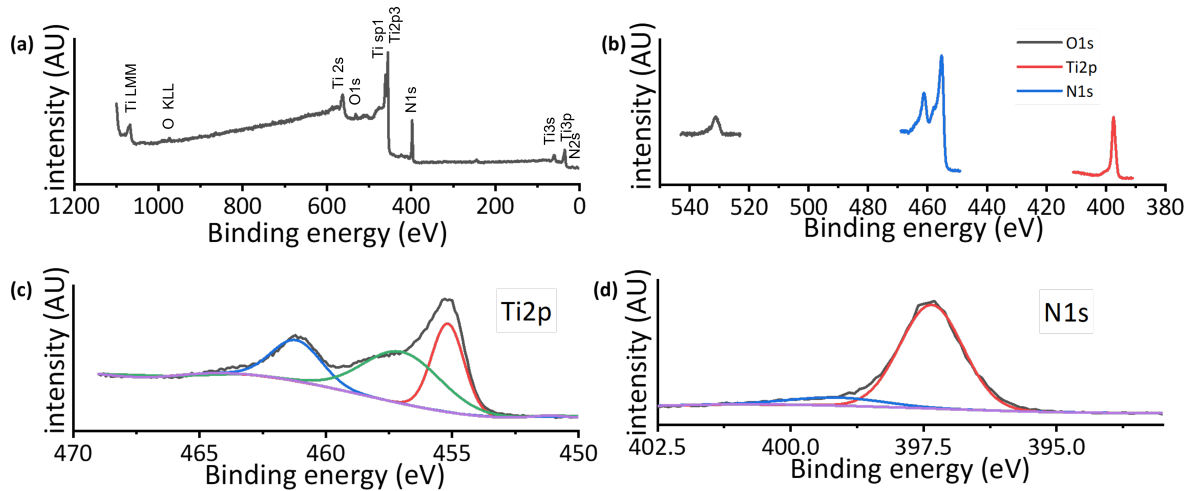


FIG. 4: XPS results of the TiN sputtered under 800 °C and 15 W substrate bias, (a) survey scan contains Ti 40.3 %, N 43.6 % and O 16.1 %; (b) high resolution scan of Ti, N and O; (c) high resolution scan result of Ti2p with three fitting peaks; (d) high resolution scan result of N1s with two fitting peaks

XPS was performed on PHI VersaProbe 3. Before the scan, a 30 s argon ion sputtering was applied to remove surface contamination. A survey scan was performed first as Fig. 4 a), followed with high resolution (HR) scan at oxygen, nitrogen and titanium as Fig. 4 b). The survey scan displayed there was mostly Ti and N in the film. However the HR scan showed there was 16.1 % O, with 40.3 % Ti and 43.6 % N. The Ti peaks consisted a Ti2p1 peak at 455 eV and a Ti2p3 peak at 461 eV, caused by Ti-N bond, with an extra satellite peak in Fig. 4 c). The N peak from the Ti-N bond is located at 398 eV as may be seen Fig. 4 d), although there is a mild minor peak of N1s at 400 eV due to N-O bonds.

Combining the results of XRD and XPS, it proved that we deposited a TiN film with extremely low resistivity, which can be used for our next device fabrication.

III. FILM PROCESSING

A. Lithography

As described in the motivation section, our process requires the ability to robustly pattern features approaching the observed limits of the *heidelberg* direct-write lithography tools commonly used in the SNF. Specifically, we required feature sizes of approximately $1\mu m$ at a pitch of approximately $2\mu m$ to achieve the desired emissivity peaks. Our high quality TiN films proved to be challenging to pattern lithographically even using standard SNF recipes.

To begin with, we had a reasonably short etch after our litho (just $100nm$ of TiN) meaning that even a $1\mu m$ resist film would still be adequate even with a selectivity of 0.1. As such, we chose to use the SNF standard $1\mu m$ SPR-3612 recipe, consisting of the following steps:

- Pieces were baked at $115C$ for three minutes to remove any adsorbed moisture. (Resist adhesion was not observed to be an issue, so HMDS vapor priming was foregone).
- SPR-3612 was spin-coated at $5500RPM$ for 40 seconds, resulting in a nominally $1\mu m$ thick film.
- The SPR-3612 was exposed using a dose and defocus which were found to adequately transfer the pattern in dose testing.
- A 60 second, $115C$ post-exposure bake smooths out the written pattern.
- The chip is gently agitated in MF-26A developer for 40 seconds.

Initial films patterned in this manner behaved as expected, with the nominal $1\mu m$ features at a $2\mu m$ pitch being well resolved as may be observed in Fig. 5. It is worth noting that the devices appeared to come out much better when patterned along the direction of *heidelberg's* motion (that is, the grating patterned vertically), whereas nontrivial line edge roughness appeared when patterned orthogonal to it, as may be seen in the indicated features near the top of Fig. 5 a).

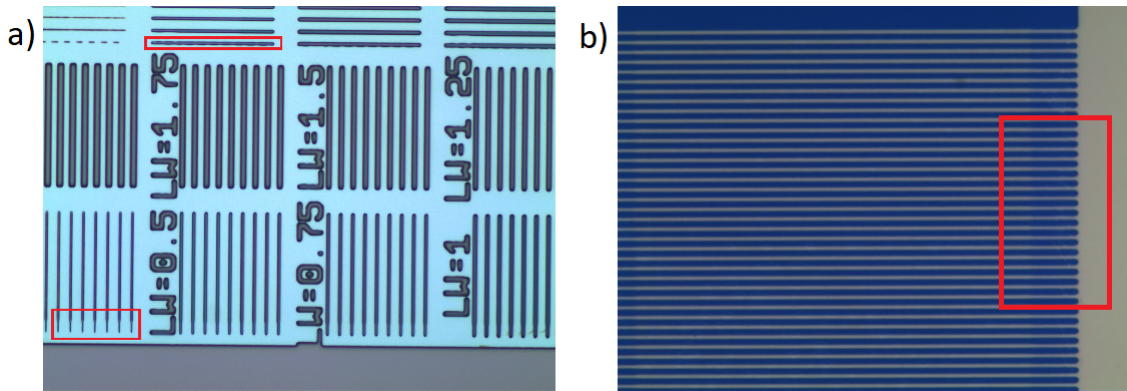


FIG. 5: Initial attempts at patterning TiN films. Dose: $55mJ/cm^2$, defocus: 2. Boxes indicate necking at edge of features and increased line edge roughness patterning orthogonal to *heidelberg's* motion. a): dose test showing variety of line widths at a $5\mu m$ pitch. b): patterned film with $1\mu m$ line width and $2\mu m$ pitch.

An additional slightly odd feature was apparent necking of the gratings near the edge of the contact as indicated in both Fig. 5 a) and b). It is unclear if this results from issues with *heidelberg* itself or rather is an effect of diffraction. The latter seems somewhat unlikely as we would expect this region to be underexposed rather than overexposed. To identify if it was some sort of turn-on artifact associated with the edge of a patterned region, a slot was added at the edge of the grating, though this was unsuccessful. We also performed a pseudo-OPC procedure where the edge gradually narrows into the grating. This proved somewhat helpful.

A wide range of dose and defocus values appeared to work adequately, meaning more careful analysis was necessary to pick the optimal parameters. In this case, the primary concern was being able to predict how a patterned width would translate into a physical device width. We would in general expect the measured width to be some affine function of the patterned width; that is, $W_{\text{meas}} = aW_{\text{pattern}} + b$ for some a and b which could be experimentally determined. As such, we chose the dose which best respected this relationship, as calculated by the dose with the lowest mean-square-error in a least-squares fit of a linear trendline.

To process the dose test, high resolution images were taken of all doses. From there, an image processing pipeline would identify the remaining photoresist using a hue-saturation-value threshold, and the width was measured as the width in pixels of the minimal bounding box. This is schematically shown in Fig. 6 a), where the red boxes represent the extracted bounding boxes. In this scheme, the dose of $55\text{mJ}/\text{cm}^2$ and defocus of 2 yielded the best linearity as shown in Fig. 6 b). Somewhat curiously, the oscillations about the patterned width were quite similar for all doses; it is likely that these are due to the discretization of the patterns into *heidelberg1*'s 100nm pixel size.

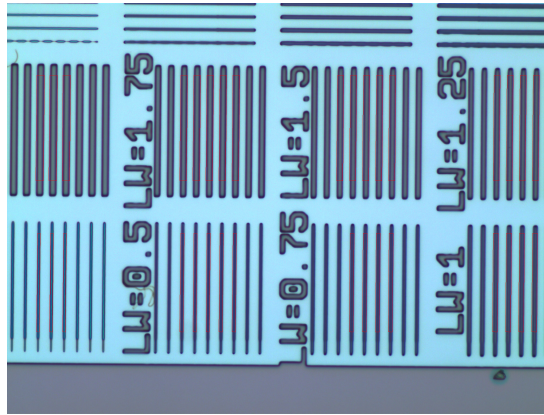


FIG. 6: Extraction of optimal dose. a) Figure showing extraction method from image. After identifying resist via a binary filter, minimal bounding boxes are drawn for each line width. The width of these boxes in pixels was used as the measured width. b) Measured width in pixels vs patterned width for the best dose of $55\text{mJ}/\text{cm}^2$ at a defocus of 2.

More severe problems arose when trying to pattern our final films, the results of which may be seen in Fig. 7. There are a few possible causes:

- Something changed in the litho procedure. Perhaps the resist or developer was contaminated; maybe something in *heidelberg* came out of alignment (somewhat unlikely, given that both given that two options were attempted for each).

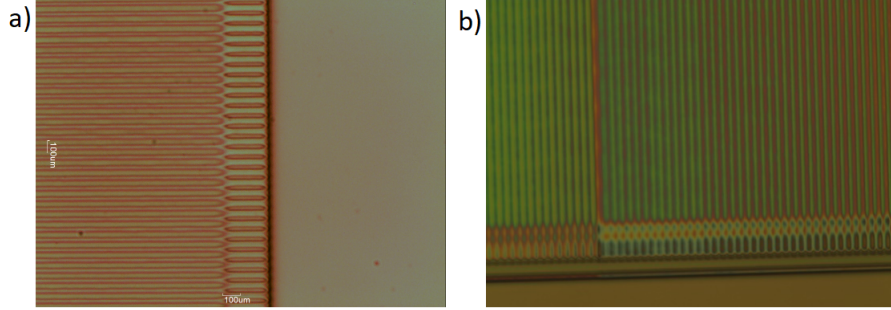


FIG. 7: Lithography troubles. a) Grating pattern appeared to be entirely inverted near the contact region. b) After adding BARC, dose/defocus values which worked well in the dose test failed to fully expose some regions while overexposing others.

- The optical properties of the TiN dramatically changed across our deposition optimization, and the optimized film is far more reflective, potentially causing issues.
- The surface roughness of the films increased due to the larger grain size. This in turn scattered light more diffusely, again damaging our ability to pattern the film.

To attempt to counteract the second two options, a back anti-reflective coating (BARC), AZ-BARLi II, was explored. This, unfortunately, was also unsuccessful, as maybe seen in 7 b). It is unclear if this was because the problem was not one a BARC layer could solve, an inappropriate recipe was used, or the BARC had exceeded its shelf life. This issue remains to be solved; in the mean time, we proceeded with somewhat coarser features than desired.

B. Etching Optimization

As a ceramic, TiN is very hard. While this mechanical stability is desirable for the longevity of a MEMS device, it does present challenges to etch with high selectivity and anisotropy. Overetch into the SiN_x under the TiN also modifies the dielectric environment and therefore the optical properties. Meanwhile, slanted sidewalls would add an additional offset to our patterned width and degrade the optical properties of our gratings. To this end, an additional DoE run was performed to optimize the etch parameters in the inductively coupled plasma (ICP) reactive ion etch (RIE) tool *PT-MTL*. Based upon our literature survey, it seemed that TiN films were typically etched in some combination of Ar and Cl_2 . Four key variables were identified:

- The pressure affects both ion/radical generation within the gas as well as the mean free path. In principle, we would expect that lower pressures should increase mean free path, hence increasing ion bombardment and etch directionality. However, this the increased physical etching will also reduce selectivity.
- The substrate bias also increases ion bombardment on the sample. Higher substrate bias should result in more anisotropic etches but also worse selectivity due to the increased physical character of the etch.
- The Ar/ Cl_2 ratio provides yet another mechanism for controlling anisotropy versus selectivity. Higher Cl_2 percentages should increase the chemical aspect of the etching,

improving selectivity. However, [1] found that some percentage of Ar was necessary to achieve steep sidewalls.

- The ICP power controls the quantity of ions and radicals. While it would most likely primarily affect the etch rates, not the selectivity or directionality, it was still included as a free variable to optimize.

In order to rapidly characterize etch conditions, chips were bonded to carrier wafers using Sandvik oil to ensure an adequate thermal interface. The etch rates in SiN_x were evaluated by using a Nanometrics Nanospec reflectometer, an optical thickness measurement tool, on the chips before and after. Meanwhile, some resist was spun onto the TiN pieces and the step height was measured via profilometry. Finally, etch profiles were evaluated by performing atomic force microscopy (AFM) on the step edge. With a half-angle of 20 degrees, this should be adequate to measure steps up to 70 degrees.

The tests ended up being somewhat inconclusive in so far as JMP did not extract any statistically significant relationships between the input conditions and the output responses. The results of this analysis for selectivity (defined as the ratio of the etch rates in TiN and SiN_x) and anisotropy (characterized by the sidewall angle) are shown in Fig. 8 a) and b) respectively. While the data is not statistically significant, we do trust some of the identified correlations given their match to our insight into the physics of the etching process. First, increased substrate bias leading to increased anisotropy and decreased selectivity is essentially a textbook response. Second, increasing Cl_2 concentration leading to increased selectivity also matches our expectations, while the improved anisotropy is plausible. Finally, limited impacts from ICP power and pressure are also both reasonable, but additional testing should be performed to verify this especially after optimizing the other parameters.

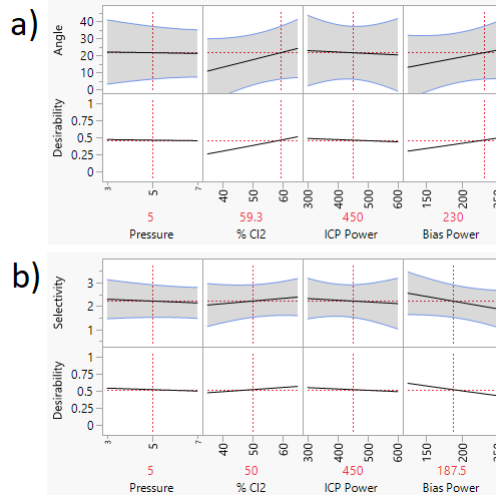


FIG. 8: JMP analysis of etching conditions. a) JMP estimate of parameter effects on etch sidewall angle. b) JMP estimates of parameter effects on etch selectivity.

While we ran out of budget to perform additional optimization based upon these findings, we did come away with two adequate etch recipes. First, if selectivity to SiN_x is the most important characteristic, an etch at 7mTorr , 65% Cl_2 , 600W ICP power, and 125W bias power resulted in a selectivity over 3.7. However, the sidewall angle of approximately 6.1 degrees was relatively poor. On the other hand, if directionality is more important, an etch

at $25mTorr$, 65% Cl_2 , 1000W ICP power, and 400W bias power achieved a sidewall angle of 46 degrees. The downside was a poor selectivity of around 0.55. A 3D view and the line cut of the AFM scan of this etch is shown in Fig. 9. Finally, the conditions of $7mTorr$, 65% Cl_2 , 600W ICP power, and 250W biasa power resulted in an acceptable compromise, with a sidewall angle of 38.8 degrees and a selectivity of 2.1. In the future, we hope to apply our findings to further optimize these etches. The input parameters and resulting sidewall angles/selectivities are shown in Table II in Appendix A.

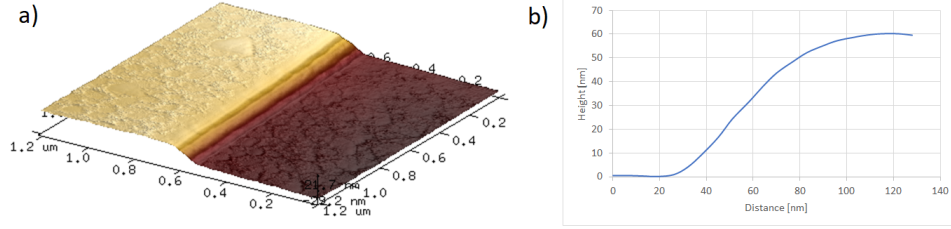


FIG. 9: Topography of etch sidewall a) 3D map of step edge. b) Line cut of steepest step edge. Note that only the top $40nm$ is TiN.

IV. DEVICE FABRICATION

After identifying functional deposition parameters and etching parameters, we could begin fabricating microheaters to verify their performance.

A. Process Flow

In general, device fabrication could be split into the the broad steps of substrate preparation, TiN deposition and patterning, and interconnect patterning (which will be referred to as "back end of the line" (BEOL) from here on). The choice of substrate has previously been discussed, as well as deposition and etching conditions for the TiN film. The complete process is shown in Fig. 10.

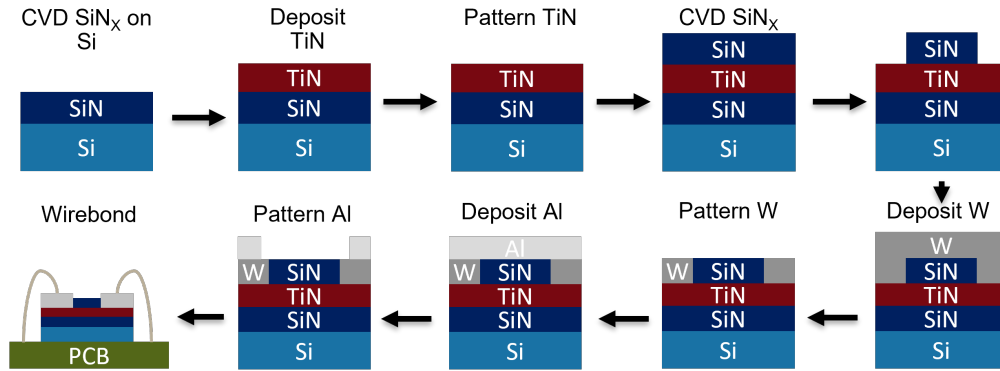


FIG. 10: Schematic of complete device fabrication flow.

The first challenge after the TiN etch was the resist burning which occurred during the etch. Specifically, traditional resist strip solvents such as acetone and heated Remover PG

were unable to remove the strings of burnt resist as shown in Fig. 11. Previous TiN films sputtered in the SNF were incompatible with the O_2 plasma strip which would typically be utilized in this case as they were oxidized in the process, increasing the resistivity and degrading the optical properties. Our optimized depositions showed sufficient robustness to remain unaffected by an O_2 plasma strip as suggested by visual inspection and resistivity measurements. However, XPS analysis should be performed before and after the plasma strip to verify this conclusion. Heated SRS-100 is a stronger solvent which may be capable of stripping the resist without any negative consequences.

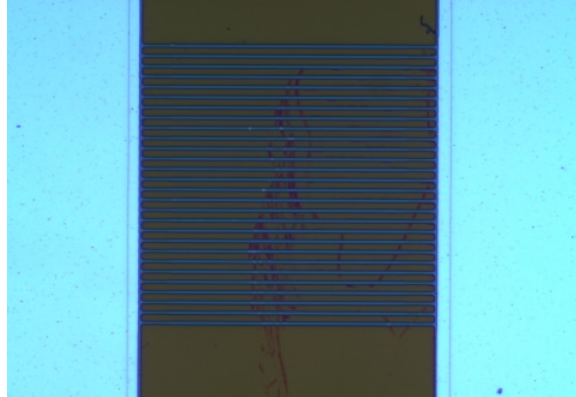


FIG. 11: Image of grating after etch and solvent resist strip showing stringers of remaining photoresist.

After removing undesired organics, an additional capping layer of PE-CVD SiN_x is deposited. This should protect the TiN grating from degradation both in the following processing (e.g. the W etch) and during its high-temperature operation where it is more vulnerable to oxidation. Next, openings are etched into the SiN_x for making contact to the underlying TiN at the edge of the grating. If we are unable to resolve the necking at the edge of the grating, we can simply extend the contact region past to the well formed middle of the grating. As the feature definition with this etch is largely unimportant, the standard SNF $1\mu m$ SPR-3612 recipe exposed at a dose of $70mJ/cm^2$ and defocus of -2 is adequate. A pre-existing CH_3F/O_2 etch measured to have an etch rate of $2.8nm/s$ is utilized.

At this point, an initial interconnect layer of tungsten is deposited and etched. Given that the interconnects will be on the order of 20-30 times longer than the grating length itself (must span a $\approx 10mm$ chip, compared to a $400\mu m$ grating), they must have a lower sheet resistance to avoid excess parasitic losses even if they are somewhat wider than the grating itself. Initially, aluminum was selected for its high deposition rate and low resistivity. Somewhat predictably, the aluminum near the heater melting during operation as may be seen in Fig. 12. As such, moving forward we shall use tungsten for its high melting point in the region around the heater itself. As the topography of this etch is unimportant, it should be designed to optimize selectivity to the underlying SiN_x . It would be simplest to use a hydrogen peroxide wet etch.

Finally, an additional Al interconnect layer is added somewhat recessed away from the edge of the heater to prevent melting. It has higher conductivity and deposition rates than tungsten, allowing us to make effective interconnects much faster. Additionally, its soft surface is possible to wirebond to, enabling us to connect our devices to external electrical test equipment. Again, a wet etch is the method of choice for patterning given the loose

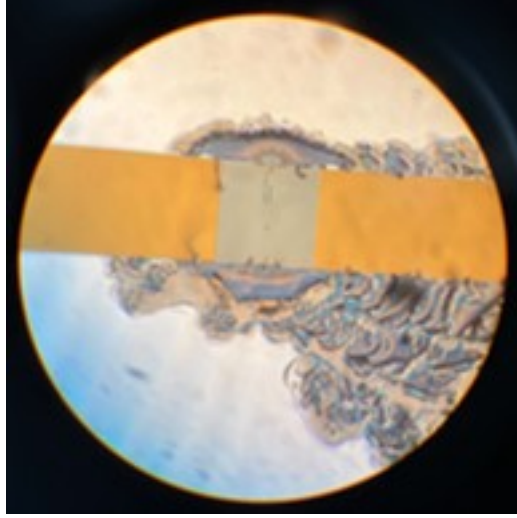


FIG. 12: Image of interconnect Al melting at the edge of the microheater.

required tolerances.

Finally, in the future we will fabricate arrays of microheaters which may be individually controlled. As such, we will need more high-current signal lines than a single interconnect layer allows for. As such, we can add additional interconnect layers using the processes we have designed here. Specifically, we can deposit another SiN_x layer, open vias, and deposit and wet etch Al interconnects.

B. Fabricated Devices

To facilitate layout of gratings with various dimensions, a kLayout parametric cell (P-cell) was defined as shown in Fig. 13. The P-cell is parametric with respect to the structure width, length, line pitch, line width, and optional pseudo-OPC triangle height.

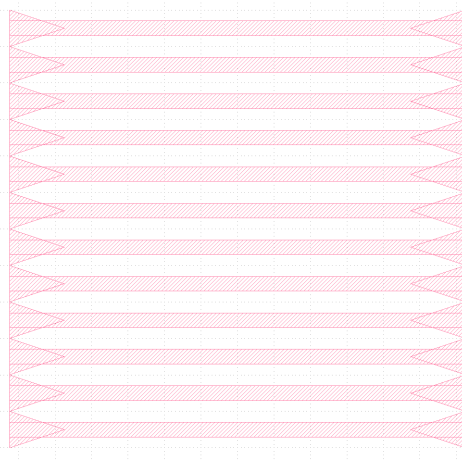


FIG. 13: Example layout of optical grating P-cell.

Additionally, real-time evaluation of temperature is important to ensure consistent emissive performance. In this application, utilizing the temperature coefficient of resistance of

the TiN grating as a variable resistor which can be measured and correlated to temperature is a natural choice. To this end, three four point probes are included in in our initial layouts to assist in determining temperature as shown in Fig. 14 a). The first device, patterned in the middle, should be at the peak temperature of the microheater. Further, it includes all four pads to drive a current and measure voltage. However, the connections to it cut the interconnect which powers the microheater in half, resulting in increased resistance and a less uniform current distribution. A second four point probe patterned at the top mitigates this issue by being at the edge, allowing for a continuous interconnect. However, it may be at somewhat less than the peak temperature, and characterization will need to be done to determine how this temperature relates to the peak temperature. Finally, the third four point probe patterned at the bottom of the device does not include a separate current drive from the rest of the grating. As such, it relies on current distributions in the microheater remaining roughly uniform. This allows us to reduce the number of signal lines and simplifies the drive circuitry. The produced layout is shown in Fig. 14 b).

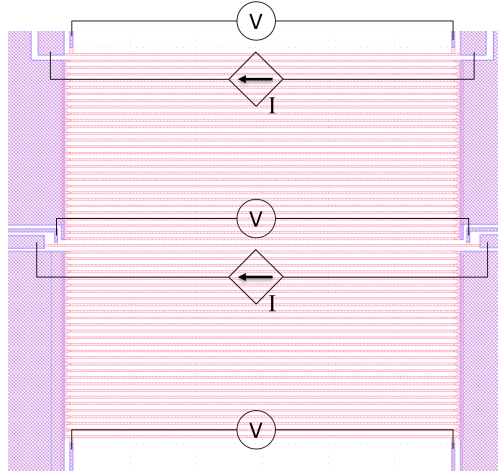


FIG. 14: Layout of one of the test microheater devices. The voltmeters and the current sources required to operate the three four point probes are schematically shown.

After fabrication, the devices had to be connected to the external drive circuitry. This was achieved by wirebonding the aluminum interconnects to a PCB which could be soldered to. The full setup is shown in Fig. 15, where the measured 141Ω shows that the microheater does exhibit continuity. Further, the parasitics caused by the interconnects and wirebonds are small compared to the heater resistance (on the order of a few ohms).

V. DEVICE CHARACTERIZATION

After completing device fabrication, we began initial characterization of device performance.

A. Emissivity Testing

First, we wished to validate the stability of the emissivity of our devices as a function of temperature. The test sestup consisted of pointing a FLIR camera at a hot plate with a



FIG. 15: Substrate with microheaters attached and wirebonded to carrier PCB.

substrate placed on top. A thermocouple held to the substrate theoretically measured the true temperature of the chip. We calibrated the emissivity at a temperature of $T = 200^\circ\text{C}$, finding values of 0.202 for the bare film and 0.404 for the grating, although the latter is more likely some average of the grating along with the material around it given the small size. The value for the bare film is higher than expected; typical values for TiN at this wavelength are generally closer to 0.1. It is unclear why this is the case.

After calibrating the emissivity of the film at some specific temperature, the temperature could be varied. In principle, if the emissivity were constant, the thermocouple and the FLIR would always measure the same temperature; if the emissivity varied with temperature, then the two would fail to track each other exactly. The results of this experiment performed with both a continuous film as well as our optical gratings after emissivity calibration at 200°C is shown in Fig. 16.

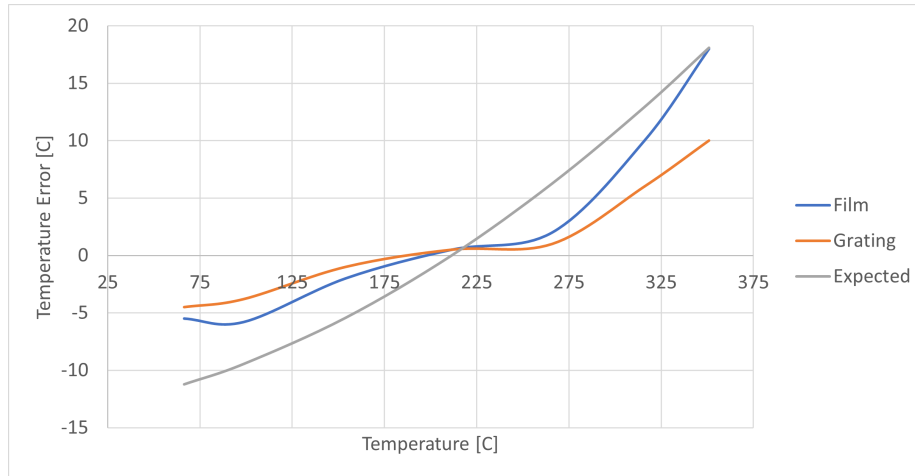


FIG. 16: The difference in temperature measured by the FLIR camera and a thermocouple after calibration at 200°C as a function of thermocouple temperature, as well as the expected plot given that approximately $0.0868\%/^\circ\text{C}$ variation in TiN emissivity from [2].

We did observe deviation which almost perfectly matches our expectations. Based upon data from [2], we might expect the emissivity to vary by about $0.0868\%/^\circ\text{C}$; assuming the FLIR calculates the temperature as $T = (\alpha/\epsilon)^{1/4}$, where α is some constant set by calibration at 200°C and ϵ is the emissivity, we calculate the trend we would expect to see, which does match our results quite well. It is worth noting that the assumption of linearity in the emissivity may not be valid, and that that data was taken at $\lambda = 1.6\mu\text{m}$ while our FLIR

integrates emissions from $3\mu\text{m}$ to $5\mu\text{m}$. A possible source of error is that there should be a temperature gradient from the film to the thermocouple held on top, a fact which would be exacerbated at higher temperatures.

B. Resistivity measurements

The other key characteristic we desired of our TiN film was a consistent temperature coefficient of resistance. To this end, we performed a similar experiment as with the emissivity measurements. Specifically, we patterned an individual four point probe with extra large pads which was then placed on a heater stage. The pads were then connected to a semiconductor parameter analyzer. The measurement setup is shown in Fig. 17.

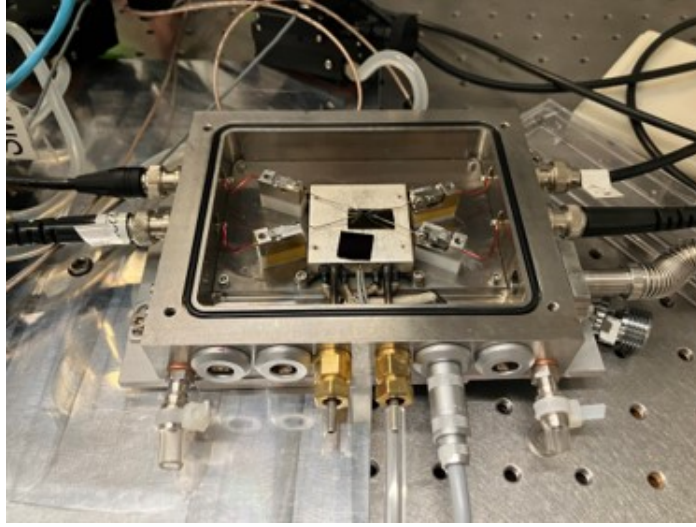


FIG. 17: The setup for the temperature coefficient of resistance measurements. The heater stage is connected to a control unit which sets the desired temperature and the four probes connect to a semiconductor parameter analyzer. The stage is capable of operating in vacuum, allowing us to reach higher temperatures without risking oxidation.

Unfortunately, the data is currently inaccessible as the computer it is on has a corrupted boot sector and the data partition is encrypted. Nevertheless, the qualitative trends are shown in Fig. 18. Up to around 250°C , the four point probe showed approximately constant resistance, implying a constant TCR as desired. However, upon heating to 330°C , the current showed an approximately exponential turn-on. Additionally, after cooling back to 250°C , the linear behavior returned. We consider it unlikely that this is actually the IV characteristics of the four point probe itself; more likely, some thermally assisted transport mechanism through the underlying dielectric is at play. To test this, we will also deposit and pattern four point probes on a wafer with a thermal oxide grown on it. This should exhibit greater resilience to breakdown when compared to the potentially low quality PE-CVD SiN_x .

C. Pulsed Measurements

As discussed in the motivation section, ultimately we wish to switch these microheaters at a high frequency. To this end, we designed drive circuitry to operate the heaters in pulsed

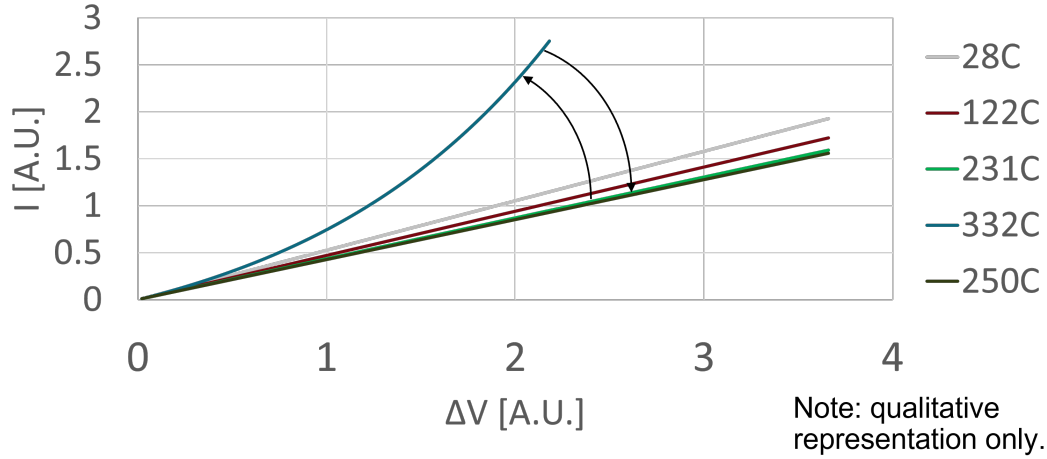


FIG. 18: A qualitative recreation of the TCR data captured; the actual data is inaccessible. Data taken in the order shown in the legend.

heating condition. The circuit diagram is shown in Fig. 19 a), and the breadboarded design is shown in Fig. 19 b). The microheater is hooked up to an external power supply with a sense resistor and a low-side NMOS FET to switch it. Two differential amplifiers amplify and attenuate the signal across the sense resistor (proportional to the microheater current) and the voltage across the load resistor respectively to scale them to the desired range.

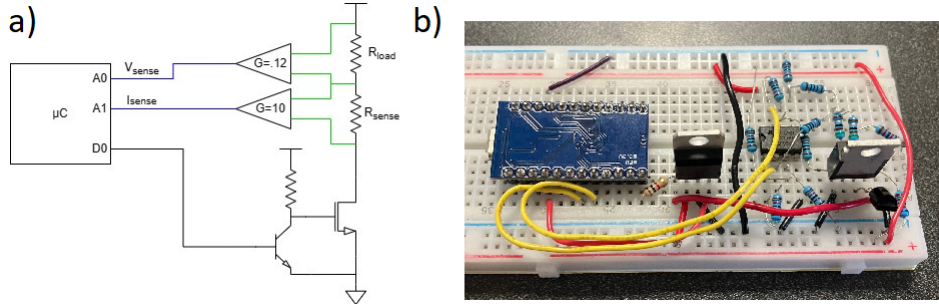


FIG. 19: Pulse circuitry. a) Schematic representation of pulse circuitry. b) circuit after construction on breadboard.

After completion of the circuit, we calibrated the voltage and current sense readings against an electronic load (E-load) in place of the sense resistor. Again, we expected the some affine function for both. The results of this are shown in Fig. 20. While some nonlinearity exists for low voltages/currents, most of the readings are well described by an affine function. In the future, this system should be upgraded with higher quality components, and a gate driver should be outfit on the low-side FET for a more abrupt turn-on.

Next, we were able to drive the microheaters with our pulsed setup and record the current and voltage as a function of time. The results of this investigation are shown in Fig. 21. We observed a somewhat anomalous resistivity curve in which the resistivity initially decreases as the power was ramped up before beginning to increase. It is unclear if this change was an effect of the increased applied voltage or the increased temperature. The heater burnt out before we were able to investigate, as at this time our substrate was simply double-sided-

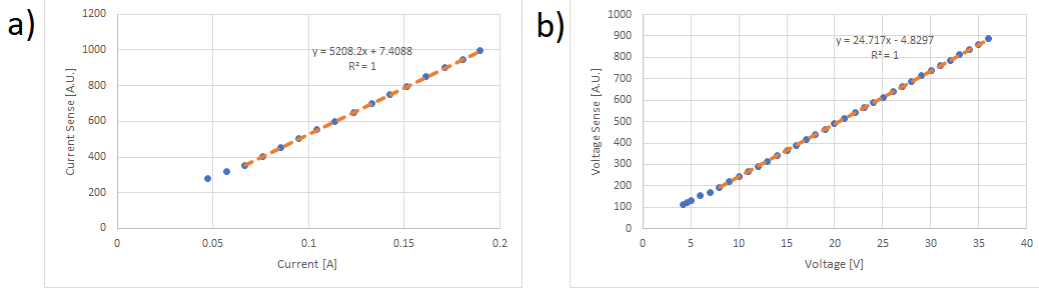


FIG. 20: Pulse circuitry calibration. a) Current sense reading vs. current measured by E-load. b) Voltage sense reading vs. voltage measured by E-load.

sticky-taped onto a carrier PCB which was not designed for heat sinking, allowing the entire substrate to heat. Going forward, we will use a high thermal conductivity epoxy to bond our device to a PCB designed to transfer heat into a mount plate.

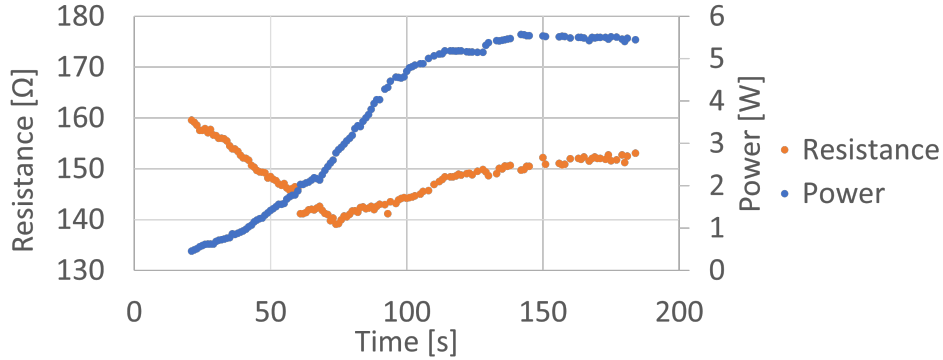


FIG. 21: Power and resistivity data measured from pulsed operation of microheater as a function of time. The duty cycle was 5% and the period was 1 second.

In the future, we wish to better understand the transient thermal response of our heaters. As such, taking high-speed measurements of the four point probes (e.g. with an oscilloscope) across heating cycles will help us understand heating and cooling rates. This should require minimal changes to our setup; we just need to add a current source for the four point probe and the oscilloscope.

VI. CONCLUSIONS AND FUTURE WORK

This project developed a recipe to deposit TiN films approaching the limit of PVD films found in literature. Further, we developed processing techniques for those films achieving reasonable selectivities and anisotropies. These processes were employed to fabricate microheaters which we began initial characterization of. As such, all of the critical objectives of the project were met. However, significant future work remains to be done, broadly split into direct improvements of this work and future extensions. The main steps for the former are listed below in addition to the discussion in the relevant sections.

- The etch anisotropy should be further enhanced using the learnings from our DoE process.

- The lithography challenges should be resolved.
- The origin of the anomalous temperature dependence on the IV curves of the four point probe should be determined.
- Transient characteristics of the microheaters should be determined.

At this point, the microheaters will be adequately characterized for integration into a larger system. This will involve emissivity measurements of various gratings in order to improve our understanding of the relationship between the patterned geometry and the resultant optical properties. The microheaters may then be utilized in parallel for gas sensing at different wavelengths.

VII. BUDGET

In total, this project cost \$4727.98. A breakdown of the costs is shown below.

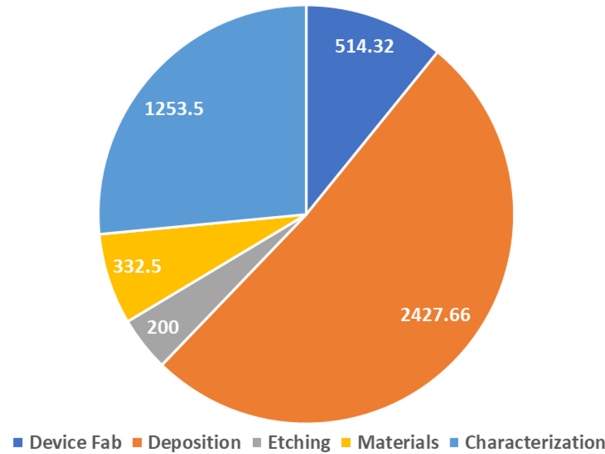


FIG. 22: Breakdown of expenses for this project by general category.

VIII. ACKNOWLEDGEMENTS

We would like to extend our gratitude to our mentors Don Gardner and Lavendra Mandyam for guidance throughout this process. Their wisdom allowed us to short circuit to conclusions which otherwise would have taken significant time and expenses to reach. We would also like to thank the all SNF and SNSF staff members for tool trainings and productive discussions. Finally, we would like to thank Chenghao Wan for assistance in device design and measurement setup.

Appendix A: Etching DoE Results

Pressure [mTorr]	Cl ₂ %	ICP Power [W]	Bias Power [W]	Sidewall Angle	Selectivity
3	35	600	250	5.5	0.9
7	35	300	125	9.5	2.3
7	35	300	250	2.1	2.0
3	65	300	125	15.3	2.6
7	65	600	125	6.1	3.7
7	65	600	250	38.8	2.1
3	65	300	250	33.4	1.9
25	65	1000	250	9	0.55
25	65	1000	400	45.5	0.56
25	100	1000	250	42.4	0.60
25	100	1000	400	25.5	0.64

TABLE II: Etch conditions and resulting angle and selectivity.

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