Micropatterning Ion Gel Electrolyte with High Aspect Ratio SU-8 Structures

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Abstract

While Organic Mixed Ionic/Electronic Conductors (OMIEC) could serve as low-power, tunable materials in electronics and photonics, the presence of shared electrolyte among adjacent devices can unintentionally modulate the properties of neighboring devices. This project presents a method for fabricating patterned gel electrolytes to address this issue of parasitic ionic currents when integrating multiple OMIEC-based devices. To achieve this, we developed a fabrication strategy using SU-8 wells as separators between devices. The process involves direct writing of SU-8 above the devices to create vertical well walls, infiltration of the wells with ion gel electrolyte, and mild etching to remove shorts between adjacent devices. The success of this method relies on the ability to pattern thick SU-8 using the Heidelberg2 system's high aspect ratio mode. This report describes the exposure conditions, development conditions, electrolyte etch efforts, and early device characterization. During the 10-week course, we successfully patterned high aspect ratio SU-8 sidewalls and functional Electrochemical Random Access Memory (ECRAM) devices. However, further optimization of the final dry etch is required to eliminate cross talk and maintain device performance throughout the etching process.

Introduction

Motivation

The integration of organic mixed ionic/electronic conductors (OMIECs) has unlocked new opportunities in electronics and photonics by serving as a low-power, tunable material. In OMIECs, ions from an electrolyte in the presence of an electric potential can modulate material properties, such as the conductivity, throughout the bulk of the OMIEC (**Figure 1**). However, when multiple OMIEC-based devices are covered by the same electrolyte, parasitic ionic currents occur. For example, when tuning one device with an applied potential, parasitic ionic currents may unintentionally tune adjacent devices in a system with a shared electrolyte. To address this issue when integrating OMIEC-based devices, patterned electrolytes can be used to allow for dynamic tuning or reading of individual devices without such parasitic currents.

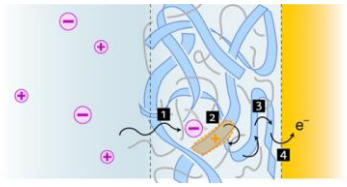

Figure 1. Mechanism of modulation in OMIEC-based devices. Ions from the electrolyte modulate properties in the bulk of the conductive polymer film. Image taken from reference [1].

Fabrication strategy

In this work, we develop a method to pattern gel electrolyte wherein high aspect ratio SU-8 wells serve as a separator between adjacent devices. In this method, SU-8 is directly written above OMIEC-based devices to create vertical well walls using the Heidelberg2. The wells created by these SU-8 structures are then infiltrated with a gel electrolyte. Finally, a mild etch is performed to remove shorts between adjacent devices. Crucial to the success of this method was the ability to pattern thick SU-8 using Heidelberg2's high aspect ratio mode. A description of this feature can be found in **Appendix 1**.

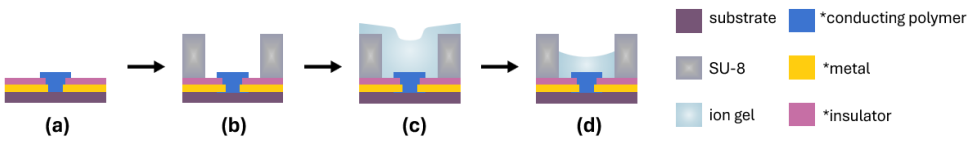

Figure 2 Fabrication Scheme. (a) OMIEC based device patterned via the germanium lift off process **(Appendix X)**. Protective germanium coating not pictured. **(b)** Direct write SU-8 on top of polymer deice to create well for electrolyte. (c) Infiltrate well with ion gel electrolyte. **(d)** Etch ion gel electrolyte to remove shorts between adjacent wells.

Method Development

Pattern Design

Two exposure patterns were used for the duration of this project. The first design was created with a test pattern, varying the dimension of wells, as well as the pitch between wells (**Figure 2(b)**). In this design, we expose everything but for the circular wells into the negative tone SU-8 resist. A pattern with Electrochemical Random Access Memory (ECRAM) (see **Appendix 4**) devices beneath SU-8 wells was also developed (**Figure 2(c))**. In this pattern, the pitch and well dimension, as well as the channel dimension of the ECRAM device were varied (**Figure 2(d)).** ECRAM devices were patterned in accordance with the germanium liftoff process, described in **Appendix 3**.

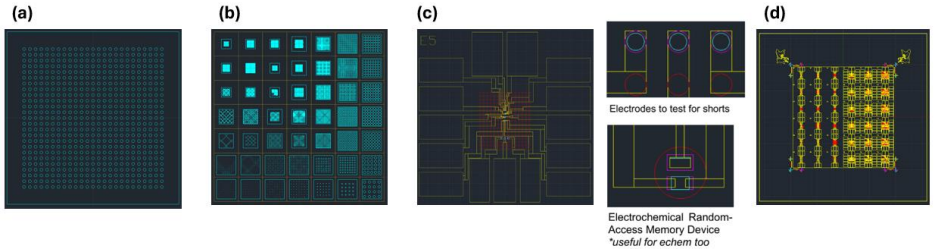

Figure 2. Layouts. (a) Example of layout to produce an array of patterned wells. **(b)** A matrix designed to vary the dimensions of the wells across columns, and the pitch between the wells across rows. **(c)** Example of layout used to pattern an array of patterned wells on top of ECRAM devices and electrodes. **(d)** A matrix designed to vary the dimensions of the wells across columns, and the pitch between the wells across rows. There is a 1 µm well with a 2 µm pitch, to 50 µm well with a 100 µm pitch.

Sample Preparation

To conserve resources over the course of multiple exposures and developments, our substrate was diced into pieces. Si wafers with 300 nm thermally grown SiO_2 were cleaned by soaking in a 120°C mixture of sulfuric acid and hydrogen peroxide (9:1) for 20 minutes. Wafers were vapor primed with HMDS and coated with 1.6 µm SPR 3612 photoresist using coat tracks (*svgcoat2*) to protect from debris from dicing. Wafers were diced into 20 mm x 20 mm pieces using DISCO wafer saw. Photoresist was removed by soaking in two baths of Remover 1165 for 1 minute each, washed with DI water, and dried with N_2. Prior to use, substrates were coated with HMDS under vacuum at 150°C in YES oven to ensure adhesion of SU-8 photoresist. Although the SU-8 manufacturer states HMDS coating isn't critical, we found that our structures were less likely to lift off during development with HMDS.

Coating pieces with SU-8 was done with caution because of significant risk for cross contamination; SU-8 is a negative photoresist and when polymerized, it is barely soluble in typical cleanroom solvents. Hotplates must be protected with a thin material to prevent transferring SU-8 onto the backside of samples. Initially, aluminum foil was used to cover the hotplate; however, this resulted in non-uniform heating because its high flexibility and light weight make it challenging to keep it in direct contact with a hot plate when heating small pieces. This non-uniformity became

apparent by the significant variation in patterned samples. One common solution is to use a metal tray; however, we used a 300 µm double side polished (DSP) Si wafer because it can be cleaned with dry etches or hot piranha. When heated to 95°C on a hot plate, the DSP wafer surface measured 1° below the set temperature.

To achieve desired thicknesses, SU-8 3010 was spun at rates according to the manufacturer's data sheet[2] ~10 µm chips were spun at 3000 RPM for 36 seconds with a 300 RPM ramp on the Laurel-R spin coater. Edge bead removal (EBR) is required on all SU-8 samples because the thicker edge can come into contact with the Heidelberg lens. A 2-3 mm EBR was done using a cleanroom swap coated in EBR PG solvent. Because of the rectangular shape of our chips, performing EBR while spinning is not feasible. However, because EBR PG has a relatively high boiling point the solvent swells the photoresist beyond the inner edge of the removed section – an effect that leads to undesired distortion of patterns near the edge. To combat this, a steady stream of nitrogen gas was blown across the chip as EBR PG was being used. Chip backsides were cleaned with EBR PG soaked swabs, dried with N_2, and carefully examined to make sure the back was pristine. After edge and backside of chips contained no visible SU-8, they were soft baked at 95°C for 3 min. Extra care was taken to ensure that chips remained level during the entire pre-exposure process because SU-8 reflow happens rapidly and can lead to thickness variation. **Figure 3** shows how the reflow distorts the photoresist near the edge of the bead removal even when the sample is kept flat. This significant reflow places a limit on how close patterns can be placed to the edge of the reflow. Our final design had no SU-8 patterns within 5 mm of each edge, and removed edge beads were kept under 3 mm.

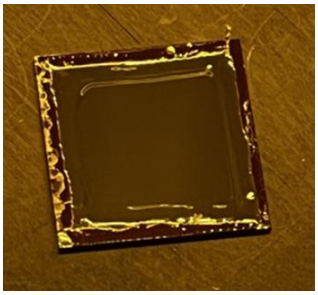

Figure 3. 20 mm piece with EBR. 13 µm thick resist with ~3 mm of an edge bead removal. On this sample, significant reflow is observed after the EBR. It was confirmed, by microscope, that the observed thickness variation was reflow and not swelling so that there wasn't risk of contaminating the Heidelberg lens.

Exposure Tests

The high aspect ratio mode decreases the entrance pupil of the light in order to increase the depth of field, thereby exposing into a larger bulk of photoresist. As a consequence of this narrower aperture, higher doses are required when utilizing this mode. Additionally, the increased depth of field makes the selected defocus less significant.

Exposure conditions should be matched to intended feature size and development condition. To understand if a feature was properly exposed, we looked at the discrepancy between the intended

pattern and the resulting dimension. As we would expect, the diameter of the well decreased as we increased the dose due to overexposure. Across the doses measured for this development condition, it appears that 2500 mJ/cm^2 is most ideal for 50 um wells, 4600 mJ/cm^2 is the most ideal for 20 um wells, and 3200 mJ/cm^2 is most ideal for 10 um wells. There is no obvious trend relating the size of the well to the optimal exposure dose, which could be a result of a small sample size.

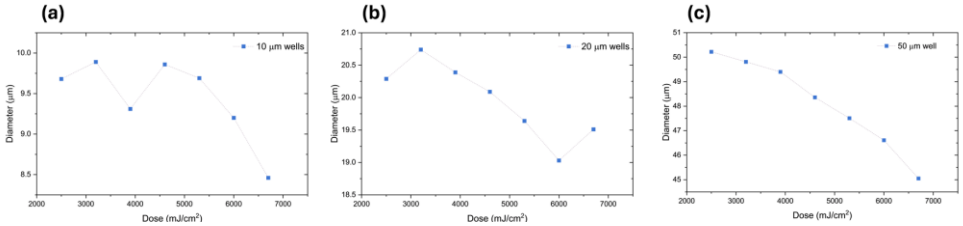

Figure 5. Intended pattern vs exposed pattern. (a) 10 um well **(b)** 20 um well (c) 50 um well. All exposures were developed for 7.5 minutes. Diameters are based on two measurements using the Keyence optical microscope.

Development Tests

Development conditions beyond the manufacturer's recommendation were explored to ensure that SU-8 scum would not impact the performance of any underlying device. After the sample cooled from the post exposure bake, it was agitated in development for 15 seconds, and then left to sit in the development bath for either 5.5, 6.5, or 10.5 minutes. Then, the sample was rinsed in a fresh bath of developer with agitation for 10 seconds.

To understand the effect of this overdevelopment, we looked at the discrepancy between the intended pattern and the resulting dimension for the 7.5 and 10.5 minute developments. **Figure 6** shows that a longer development time results in a larger than designed dimension, while the 7.5 minute dimension results in well that is smaller than the intended design. We note that this exact dimension is heavily dependent on the exposure dose.

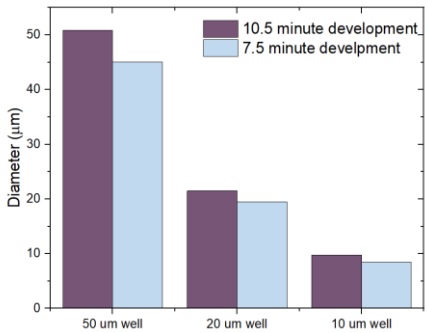

Figure 6. Diameter of patterned well. Wells were exposed with 5,300 mJ/cm^2 dose. Value is based on the average of two measurements.

The ideal development condition depends on the feature size opted for. It is clear upon visual inspection that a development condition that works for a 10 um well may result in overdevelopment of a 50 um well of the same resist thickness (**Figure 7**). We suspect that it takes longer for developer to solvate the unexposed SU-8 resist in the 10 um higher-aspect ratio feature. While not necessarily optimal, we found that a 7.5 minute development time was an acceptable condition to proceed with for the following experiments with wells of different sizes.

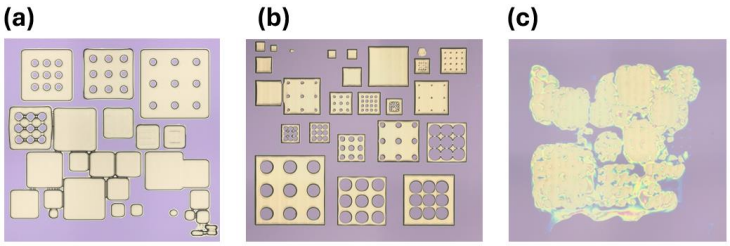

Figure 7. Images of Development Conditions. (a) A qualitive example of an underdeveloped SU-8 test structures exposed at 6,700 mJ/cm^2. **(b)** An acceptable development condition for 10 um wells that results in the overdevelopment and feature degradation of 50 um well test structures. These features were exposed with a dose of 4600 mJ/cm^2 and developed for 10.5 minutes. **(c)** SU-8 test structures that were destroyed in a 10.5 minute development, but remained acceptable in a 7.5 minute development. All images were taken using the Keyence optical microscope. The largest patterned circle is approximately 50 um.

Test device preparation

To test whether crosstalk between adjacent wells could be removed, we needed to pattern devices that could fit inside individual wells. For this purpose, we fabricated PEDOT:PSS organic electrochemical transistors (OECTs) and electrodes following an established protocol.[3] In short, instead of coating the prepared wafers with HMDS and 1.6 µm SPR-3612 for dicing, they were coated with LOL 2000 at 3000 rpm for 60s. Coated wafers were baked at 190°C for 30 min and allowed to cool. 1 µm SPR-3612 was coated on wafers and then the wafers were exposed at 65 mJ/cm^2 with –2 defocus using Heidelberg2 375 nm to pattern metal contacts and traces. Dose was chosen after performing a dose/defocus test and observing when smallest feature was approximately the correct size. Substrates were developed using standard recipe on svgdev tracks.

Ti (5 nm) / Au (50 nm) / Ti (5 nm) was e-beam evaporated with AJA and liftoff was performed by soaking wafers in Remover 1165 overnight. Wafers were rinsed with IPA, dried under nitrogen, then placed in SRD for further cleaning. 230 nm SiO_2 was deposited using HDPCVD and then wafers were vapor primed with HMDS and coated in 1 µm SPR-3612 using svgcoat. Gold contacts were exposed with Heidelberg2 375 nm using 70 mJ/cm^2 and –2 defocus. Photoresist was developed using standard svgdev recipe and SiO_2 was etched using CHF_3 on Pt-Ox.

PEDOT:PSS solution was made by mixing a solution containing 5% ethylene glycol, 1% (3-Glycidyloxypropyl)Trimethoxysilane, and 94% Clevios PH 1000 and then sonicated for 5 min.

Wafers were plasma cleaned using 10 sccm O_2 for 30 sec at 300 W in the March plasma asher in the flexible cleanroom. PEDOT:PSS solution was spincoated for 120 sec at 2000 RPM using the flexible cleanroom headway spinner. Samples were baked at 140°C for 30 min. Wafers were coated in 100 nm Ge in AJA e-beam evaporator and then vapor primed with HMDS and coated with 1 µm SPR-3612. Photoresist was exposed using Heidelberg2 375 nm at 70 mJ/cm^2 and –2 defocus. Photoresist was developed using MF-26A on the svgdev tracks. Ge and PEDOT:PSS were etched sequentially using CF_4 and a mixture of 45 sccm O_2/5 sccm CHF_3 in Pt-ox respectively. Wafers were coated with 1.6 µm SPR-3612 for dicing as previously described. Prior to use, pieces were submerged in two sequential baths of Remover 1165 for 1 minute each and then rinsed with DI water and dried under nitrogen.

Ion Gel Deposition

In this project we used an ion gel electrolyte because they are solid-state and their properties are tunable. An ion gel consists of an insulating polymer matrix that is swollen with an ionic liquid. In this work, we selected 1-ethylimidazolium bis(trifluoromethylsulfonyl)imide (EIM:TFSI) as the ionic liquid and poly(vinylidene fluoride-co-hexafluoropropylene) (PVDF-HFP) as the matrix (**Figure 8**).

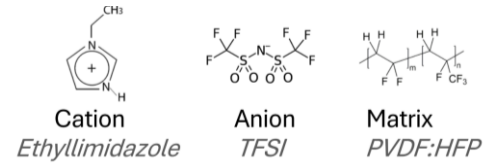

Figure 8. Chemical Structure of Ion Gel Electrolyte. EIM:TFSI (98% grade) was purchased from lolitec and the PVDF-HFP pellets with an average weight-average molecular weight of ~400,000 were purchased from Sigma-Aldrich.

The ion gels were prepared in non-SNF facilities by dissolving PVDF-HFP and the ionic liquid in acetone. We selected gels that were 80 wt % ionic liquid and 20 wt % PVDF:HFP because of prior success with this ratio. Gel solutions were made with a concentration of 45 mg of PVDF:HFP per mL of acetone. The resulting ion gel solution was stirred at 50°C for 15 minutes and then drop-cast onto the SU-8 structures with a micropipette in ambient conditions. After deposition, the structures were placed into a ~-31 mmHg vacuum that was kept at 50 °C.

Scanning electron microscopy (SEM) was used to verify that the ion gel pooled in the SU-8 wells, creating a thickness variation in the electrolyte film that would enable the etch to remove the ionic short circuits without etching the bulk gel. SEM images (**Figure 9**) show that wells sized 10 µm and below are filled with ion gel and create a flat surface, whereas larger wells contain ion gel that slopes at an angle less than 90°. Both cases reveal a thickness variation of the ion gel which can be exploited to selectively etch undesired sections of electrolyte.

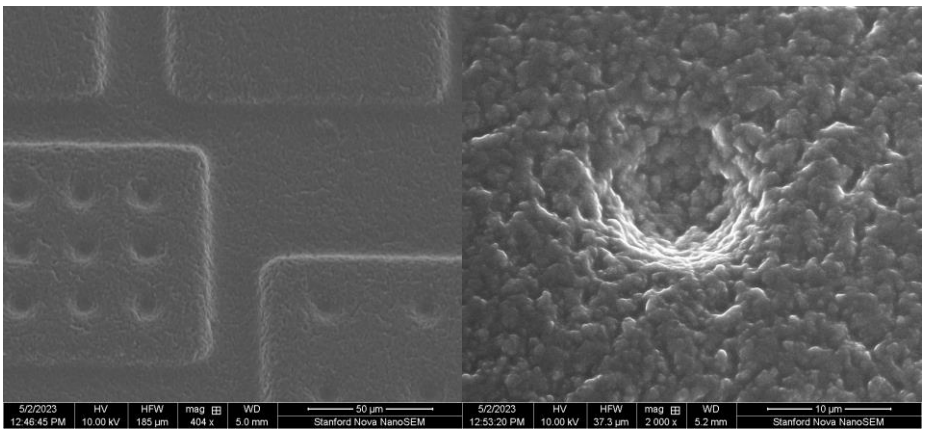

Figure 9. SEM images of ion gel coating SU-8 wells. ~5 nm sputtered Ir on surface imaged at 30° angle. (Left) Well diameters 10 µm or less are completely coated with ion gel and cannot be observed in the upper patterned squares. (Right) Ion gel pools in a 20 µm well with sloped (i.e., not vertical) edges. 80 wt % EIM:TFSI PVDF:HFP was used as the ion gel.

Ion Gel Etch

Ion gels were etched using different plasma processes. Initially SAMCO plasma etcher in RIE mode was used with 15 sccm O_2 at 300 W and etch rates were taken (Dektak profilometer) to confirm that SU-8 was not etched significantly faster than gel electrolyte (Figure 11). Although etch rates were similar, the O_2 plasma caused a significant yellowing of the gel (**Figure 10**), a common indicator of material oxidation, and the test devices showed degradation in performance.

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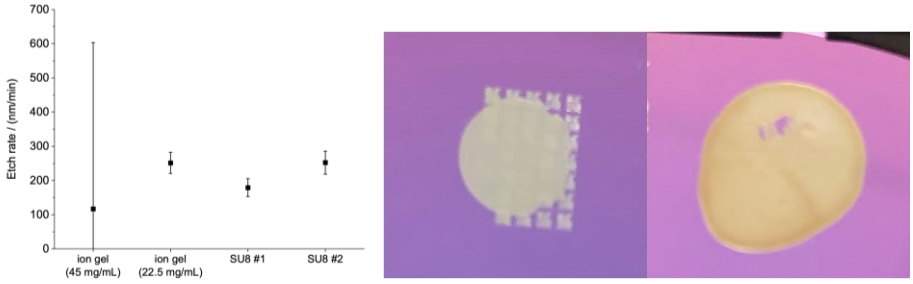

Figure 10. Ion Gel Etch. Samples etched with 15 sccm O_2 in SAMCO at 300 W on direct RIE shelf. (Left) Etch rates of different samples. 45 mg/mL ion gel sample had a thickness variation greater than the total etch depth, resulting in very low precision for rate measurements. (Middle) Unetched ion gel sample drop cast on SU-8 structures. (Right) Ion gel sample on Si/SiO_2 etched for 2 mins showing significant yellowing.

Various etch gases were screened using Pt-Ox ICP etcher to search for a gas that didn't cause observable electrolyte degredation. 5 gas mixtures were tested (CHF_3, CF_4 50 sccm, H_2/N_2 45

sccm/5 sccm, N_2/O_2 40 sccm/10 sccm, and Ar 40 sccm) and images the etched gels can be seen in **Figure 11**. The appearance of the CF_4 sample closely resembles the CHF_3 sample and thus an image is omitted. Of the gases, the H_2/N_2 was the only gas that did not cause significant yellowing of the gel and this combination was used for the remaining test devices. Interestingly, the Ar sample appeared to only turn the edges yellow, but the entire substrate was coated in a yellow film. It's possible that an Ar mixture would be viable if combined with another gas to prevent sputtering the sample, but this was not explored further.

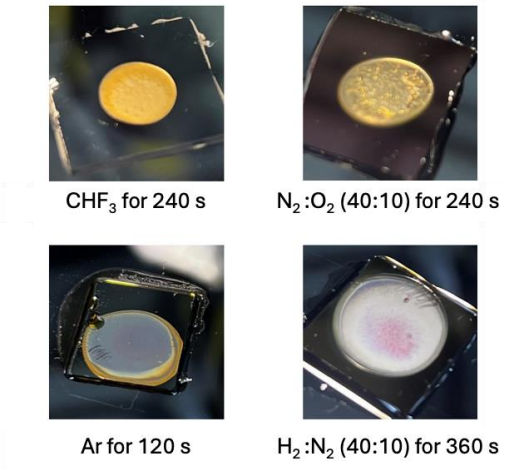

Figure 11. Images of Ion Gel After Various etch conditions.

Device Characterization

To characterize the functionality of our devices to store and isolate electrolyte, we patterned ECRAMs in each electrolyte well (**Figure 12**). We successfully wet the wells with our solid-state electrolyte and have operational devices. However, we still observe crosstalk between wells after our process.

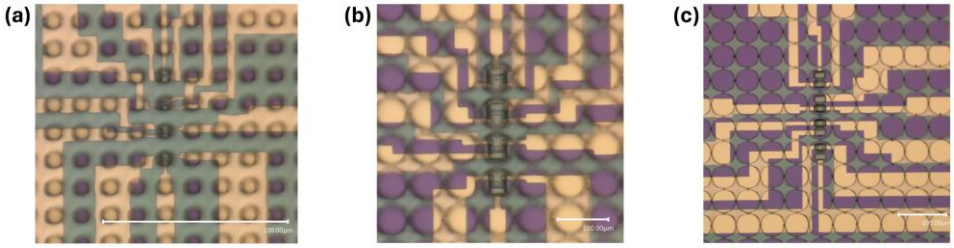

Figure 12. SU-8 wells patterned on ECRAM devices. **(a)** 10 um wells with a 2 um ECRAM channel **(b)** 20 um wells with a 4 um ECRAM channel **(c)** 50 um wells with a 10 um ECRAM channel.

The 2 um channel ECRAM devices approach the limit of devices traditionally made with the germanium lift off process. Still, it appears that we were able to fabricate ECRAM devices that were semi-operational before and after our process, as demonstrated by a transfer curve. Before our process, the transfer curve of a device gated with a gate 10's of microns away was approximately equivalent to a device gated with its own proximal gate (**Figure 13(a)**). This represents the effect of sneak currents from adjacent devices that motivate the effort to pattern electrolyte. After our process, it appeared that the distant gates were able to modulate the channel to a lesser degree than the proximal gate, indicating a possible increase in solution resistance of the electrolyte (**Figure 13(b)**). A stepped bias was applied to the devices gate and the conductance over time was measured. **Figure 13(c)** shows that there is minimal response to the first pulse but the channel achieves some level of conductance at the subsequent higher voltage pulses. This measurement was repeated, but instead the gate pulse was coming from a with a distant gate in a separate well. Together, these results indicate that there remains some degree of electrolytic shorting between adjacent wells.

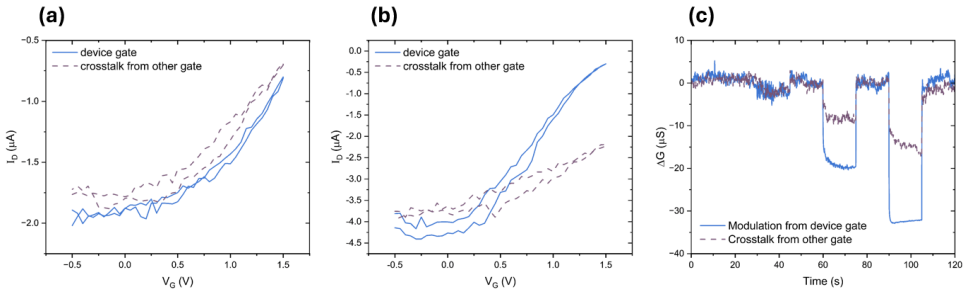

Figure 13. (a) Transfer curve of 2 um ECRAM devices before our process. **(b)** Transfer curve of 2 um ECRAM devices after our process **(c)** Change from stable open circuit conductance over time after application of 1 V, 2 V, and 3 V. For all measurements the drain voltage was –0.1 V.

The ECRAM devices with 4um channels and 20 um wells were more reliable devices and the same trend before and after our process. Before our process, the transfer curves of both the local and

distant gate were quite similar. After our process, we saw current modulation decrease mildly for both conditions, but more severely for the condition where the device was being gated by a distant gate (**Figure 14**). In the stepped measurement, we saw a conductance response to all applied biases when gating with the local gate. Using an external gate, there was also a conductance response, but this response was slower and lower in magnitude, consistent with the transfer curve. This result again suggest that solution resistance between shorted electrolytes has increased to some degree after our process.

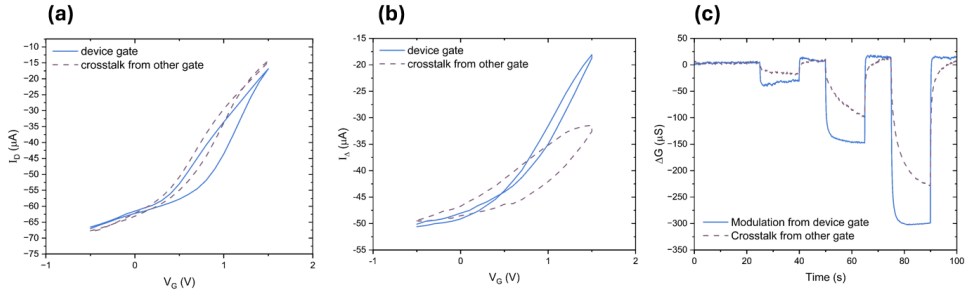

Figure 14. (a) Transfer curve of 4 um ECRAM devices before our process. **(b)** Transfer curve of 4 um ECRAM devices after our process **(c)** Change from stable open circuit conductance over time after application of 1 V, 2 V, and 3 V. For all measurements the drain voltage was –0.1 V.

Finally, these measurements were repeated for the ECRAM devices with 10 um channels and 50 um wells. After our process, we saw current modulation decrease for both conditions (**Figure 15(b)**). However, it decreased more significantly for the devices local gate, resulting in nearly equivalent transfer curve. This device was able to respond well to stepped pulses, however this modulation from an external gate was still observed (**Figure 15(C)**). In the stepped measurement, we saw a conductance response to all applied biases when gating with the local gate, as well as the distant gate.

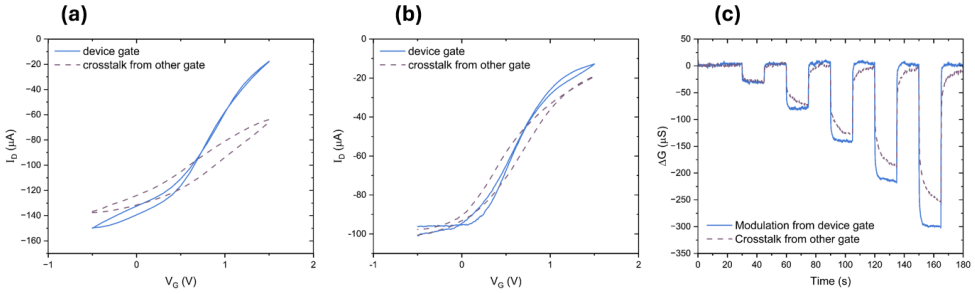

Figure 15. (a) Transfer curve of 10 um ECRAM devices before our process. **(b)** Transfer curve of 10 um ECRAM devices after our process **(c)** Change from stable open circuit conductance over time after application of 0.1 V,-0.5 V. For all measurements the drain voltage was –0.1 V.

We do want to note that these transfer curves are non-ideal and contain some amount of hysteresis both before and after our process. One theory for this non ideality is incomplete germanium removal, as the germanium oxidation step in the liftoff process was shortened.

Outlook

We report a method to pattern electrolyte wherein high aspect ratio SU-8 wells serve as a separator between adjacent devices. During the 10-week course, we successfully patterned high aspect ratio SU-8 sidewalls. However, further optimization of the final dry etch is required to eliminate cross talk and maintain device performance throughout the etching process. Moving forward, possible approaches could involve implementing a higher aspect ratio well design to enable longer etch times, which would provide better control in the etching process. Additionally, exploring the use of spin or spray coated ion gel, instead of drop casting, may achieve a more uniform film thickness. A more uniform thickness of the electrolyte would improve our ability to utilize etch rate calculations in the final etch. Finally, there is work to be done in understanding the chemistry of the interaction between the ion gel etch gas and investigating ion beam milling as a potential final etching method.

References

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[2] SU-8 3000 Permanent Negative Epoxy Photoresist Technical Data Sheet. https://kayakuam.com/wp-content/uploads/2020/07/KAM-SU-8-3000-Datasheet-7.10-final.pdf
[3] Tuchman, Yaakov. Novel methods of organic electrochemical device nanofabrication and characterization. [Doctoral Dissertation, Stanford University], 2020

Appendices

Appendix 1- High Aspect Ratio Mode on the Heidelberg2

Hidden in the Heidelberg2's process run page is a high aspect ratio feature that allows for exposure into thick photoresist. This is possible by decreasing the size of the entrance pupil of the lens (the numerical aperture), which increases the depth of field (DoF). This mode is designed for use with thick photoresist layers. It requires a higher dose, a longer exposure time, and offers worse resolution than standard exposure. Check out the nanonugget on this mode for more tips and tricks!

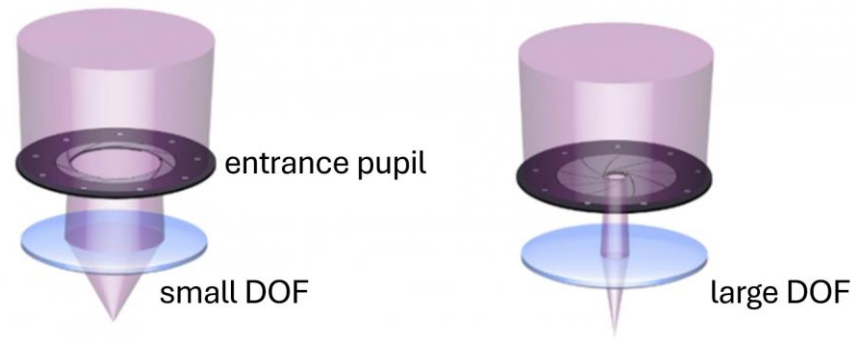

Figure A1. Graphic depicting high aspect ratio mode.

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Appendix 2- High Aspect Ratio SOP

1. HMDS Vapor Prime:

a. Place the samples in the YES HMDS vapor prime oven (*yes*) and run the standard process to dehydrate and vapor prime at 150°C.

NOTE: This step enhances adhesion between the substrate and the SU-8 resist.

2. Preparation of Wet Bench for Spin Coating:

a. Cover the hotplate with a thin material to protect from SU-8 and set the hot plate to soft bake temperature (95°C for SU-8 3010)

b. Ensure the spin coater (*laurell-R*) is ready for use by covering all actively used areas of the bench with aluminum foil to reduce the risk of SU-8 contamination.

c. Gather the necessary equipment, including a single-use pipette, bottle of SU-8, and EBR solution.

NOTE: It is advised to cut the tip of the single-use pipette to more effectively pipette the viscous SU-8.

e. Establish a plastic waste bag in the wet bench area.

3. Spin Coater Setup:

a. Program the spin coater (*laurell-R*) with the desired ramp and RPM settings.

b. Place correct chuck on spinner.

c. Place substrate in center of chuck and turn on vacuum. Check to make sure substrate is under vacuum by gently applying pressure with tweezers.

d. Press run and observe to make sure sample is centered and recipe is correct.

e. Verify the hotplate is at the correct soft bake temperature. Do NOT continue until hotplate is at temperature.

f. Open the bottle of SU-8 carefully, mindful of any particles generated by the crust on the threads.

g. Pipette the required amount of SU-8 onto the sample, careful to avoid pipetting bubbles or particles from the threads of the bottle.

4. Edge Bead Removal:

a. Once the spin coating cycle is complete and the piece is still held by vacuum to the chuck, remove the edge bead using an EBR PG saturated swab.

b. To aid the evaporation of EBR PG, gently blow the sample with an air gun while performing the EBR.

NOTE: It is crucial to remove the edge bead, especially when working with thick photoresists like SU-8 3010. Aim to remove 2-5 mm to prevent contamination of the Heidelberg2 objective. Thicker photoresists require a larger edge bead removal compared to thinner resists. You should not be able to see thickness variation at the edge except from reflow; this results in a decreased thickness at the edges which is acceptable.

c. Remove sample from chuck and gently wipe backside if with swab. Do NOT tilt sample or else there may be thickness variation because of reflow.

d. Verify that there is no edge bead, and the backside is clean.

5. Soft Bake:
a. Place the coated substrate onto the covered hot plate and bake it at the soft bake temperature (95°C for SU-8 3010) for the desired time. Look up SU-8 data sheets from Kayaku Advanced Materials to estimate time based on thickness.
NOTE: Ensure there is sufficient thermal contact between the substrate and the hot plate. Using a double-sided polished wafer or metal tray underneath the sample improves thermal contact compared to aluminum foil when working with individual pieces.

6. Heidelberg Setup:
a. Detach and carefully remove the standard chuck from the Heidelberg2 stage, avoiding hitting the objective as the stage is removed. Place the stage on a clean wipe inside of the Heidelberg chamber, at the surface above the write head
b. Insert the SU-8 specific chuck, located on a wipe on the surface above the write head. After handling this chuck, change the outer vinyl gloves.
c. Place the substrate in the center of the chuck and pull a vacuum. Test the vacuum by nudging the piece with the back edge of the tweezer. Vacuum should be maintained for further processing.
d. Once confirmed, close the window.

7. Heidelberg Exposure:
a. Create job, add a layer, and choose desired design.
b. Select the high aspect ratio mode by clicking on the resist in the selected layer settings. Then, sort the resists by Focus Depth and select either large, or extra-large. NOTE: The name of the selected resist doesn't matter. Most of the parameters are suggested guidelines and can still be changed before exposure. However, the focus depth can only be changed here.
b. When loading sample, select small substrate if laser is difficult to see. This will allow you to manually select the center of the substrate and decreases the risk of crashing the objective into the sample which can significantly damage the equipment.

8. Post-Exposure Bake (PEB):
(Optional) Before PEB, bake the substrate at a low temperature for 1 minute (65°C for SU-8 3010) to reduce thermal stress
a. After exposure, transfer the sample from the Heidelberg to the hot plate.
b. Bake the exposed substrate at the PEB temperature (95°C for SU-8 3010) for the specified duration. Look up Kayaku Advanced Materials SU-8 data sheets for PEB times.
NOTE: Again, maintain sufficient thermal contact between the piece and the hot plate.

9. Development and Drying:
a. Remove the piece from the hot plate and allow it to cool.
b. Fill out two chemical labels for SU-8 developer.
c. Inside the fume hood (*lithosolv or wbflexsolv*), fill two development dishes with SU-8 developer and add chemical labels. Cover glassware with foil.

d. Carefully pick up the cooled piece with tweezers and gently tilt the dish while agitating to ensure the entire substrate is submerged. If patterned features lift off during development, it is possible you are using too much agitation.
e. After agitation, allow the piece to sit at the bottom of the dish for the designated development time.
NOTE: depending on the intended use overdevelopment is recommended to ensure that any residual SU-8 is removed.
d. Transfer the developed piece to a fresh SU-8 developer, agitating the sample for an additional 30 seconds in this solution.
e. Dry the piece using a nitrogen gun.
Note: Be sure to label the development dishes as SU-8 contaminated to prevent cross-contamination.

10. Optional Hard Bake:
a. After development, consider performing a hard bake at a temperature 10°C higher than the anticipated operating temperature of the device.
NOTE: The hard bake is optional but is believed to anneal cracks formed within the SU-8 resist.

Appendix 3- Germanium Lift off Process Description

1. Pattern gold
a. Clean substrates using 120°C H_2SO_4/H_2O_2 (9:1) piranha hot pot on wbflexcorr. Be sure to use an insulating substrate such as thermally grown SiO_2
b. Dehydrate wafers by baking at 150-200°C for 10 minutes
c. Spin coat LOL2000 for 60s at 3000 rpm on headway2 or headway3.
d. Bake for 30 min at 190°C
e. Coat wafers with 1 µm SPR-3612 by spinning at 5000 for 60s and soft bake at 90° C for 60s
f. Expose photoresist using Heidelberg or Heidelberg2. Determine best dose/defocus by doing a dose/defocus test if necessary.
g. PEB, Develop in MF-26A, and hard bake using standard protocol on svgdev track
h. E-beam evaporate Ti (5 nm) / Au (50 nm) / Ti (5 nm) using AJA
i. Lift-off gold by submerging substrates in Remover 1165 overnight. Rinse with isopropanol and dry under nitrogen.

2. Pattern SiO_2
a. Use SRD prior to vapor deposition.
b. Coat substrates with desired thickness of SiO_2 using HDPCVD. 100's of nm is recommended to limit parasitic currents.
c. Vapor prime wafers with HMDS and spin 1 µm of SPR 3612 using svgcoat2
d. Expose using Heidelberg or Heidelberg2. Calibrate dose/defocus if necessary.
e. Bake and develop photoresist using svgdev track as done when patterning gold.
f. Open gold contacts by etching SiO_2 using CHF_3 in Pt-ox

3. Pattern PEDOT:PSS
a. Fill tube with Clevios PH 1000 and add 1% (3-Glycidyloxypropyl)Trimethoxysilane and 5% ethylene glycol then sonicated for 5 minutes.
b. Plasma treat wafers using O_2 plasma for 30 sec at 300 W (direct plate in March plasma asher in flexible cleanroom)
c. Spin coat PEDOT:PSS solution for 1 min at 2000 RPM then bake for 30 min at 140°C
d. Evaporate 100 nm Ge using AJA e-beam
e. HMDS vapor prime and coat with 1 µm SPR-3612 using coat tracks
f. Expose photoresist using Heidelberg or Heidelberg2. Calibrate exposure parameters if necessary.
g. Develop SPR-3612 resist as described above using standard recipe on svgdev track
h. Etch Ge using CF_4 in Pt-ox then etch PEDOT:PSS using O_2/CHF_3 45 sccm/5 sccm in Pt-ox.

4. Dice samples
a. Vapor prime and coat wafers with 1.6 µm SPR-3612 on coat tracks. Hard bake using svgdev tracks.

b. Dice wafers into pieces using DISCO wafersaw.
c. Remove photoresist by soaking chips in two sequential baths of Remover 1165 for 1 min each.
d. Rinse with isopropanol and dry under nitrogen.

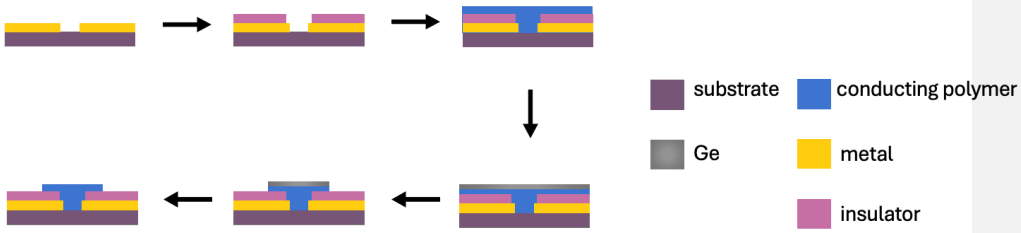

Figure A3. Fabrication scheme to pattern polymer devices.

Appendix 4- Brief ECRAM Operation

Arrays of Electrochemical Random Access Memory (EC-RAM) devices can be used to make hardware accelerators that more efficiently implement artificial neural network computation by collocating logic and memory. In an EC-RAM, voltage pulses at the gate tune the conductance (memory state) of the channel. **In Figure A4** below, we provide a schematic transfer curve and pulsed measurement to supplement the interpretation of our device results.

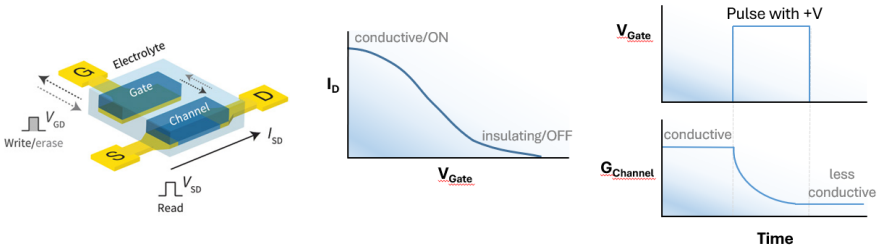

Figure A4. Operation schematic of ECRAM devices